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Trends and Challenges in Grid-Tied Inverters for Photovoltaic Applications

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Abstract Grid-Tied inverter has gained the attention of many researchers and power generation industry due to its capability of integrating distributed power generation systems using renewable energy resources with the existing centralized power generation system. Yet the inclusion of a transformer in the Photovoltaic (PV) inverter makes it bulkier, heavier and more expensive. A primary solution to the aforementioned problems is the transformerless PV Grid-Tied inverter. This paper presents a review of different transformerless, single-phase Grid-Tied inverter topologies. The objective of this paper is to study parameters such as leakage current, common-mode voltage, total harmonic distortion, and the efficiency of transformerless Grid-Tied inverters. The paper also provides a discussion on existing Grid-Tied inverter topologies, such as H5, oH5, Novel H5, H5-D, FBDC, H6D2, Hybrid H6, High-efficiency MOSFET H6, Improved H6, 3L H6, H6-A, B, High-Efficiency H6, H6-N, Improved H6, H6-active clamping, Active clamped snubber based H6, Heric, oHeric, Enhanced Heric, Heric-with mid-DC-link, Active clamping, PN-NPC, Improved FBNPC, T-Type 3L, ANPC, HBNPC, NIFB-NPCI, VNIIFBC, M-NPC, Virtual DC bus based inverter, Active Virtual Ground, Type I, Type II, Type III Common Ground, Flying Capacitor and Multilevel Common Ground. Though it is found that many topologies available in the literature, other new topologies can be proposed to improve the performance of the inverter. Furthermore, it is also noted that the performance analysis of the inverter must be carried out in the presence of junction capacitance and shoot-through problem so that new strategies can be introduced in the existing typologies to address these issues.

Keywords Grid-Tied Inverter, Transformer-less Inverter, Photovoltaic

1. Introduction

Modernization and population growth have dramatically increased energy demand. To meet this energy demand, it is important to shift towards renewable energy resources as they are abundantly available in nature, they do not disrupt with the consumption and thus saves Mother Earth. Solar energy is one such renewable energy that is never-ending and abundantly available on the earth. Thus, the production of distributed energy with solar energy has gained more prominence. It is possible to use this energy for stand-alone system (Off-Grid), grid integrated system (On-Grid) or hybrid system (the producer can store the required energy in the battery and the excess can be feed into the grid). The focal elements of On-Grid PV system that doesn't include storage battery is shown in Fig. 1. It consists of an array of PV cells that generates DC power [1]. The generated power is fed to the grid after converting it to AC power using an inverter.

The major challenges in the On-Grid systems are long lifetime, great efficiency, and good ecological circumstances. Potential challenges in the design aspects are, to decrease the size and price, reliability, complexity of inverter and also meet the standards required to inject power into the grid. To reduce the size of the system the technology has moved from transformer to transformerless inverter. In the transformerless inverter, the galvanic isolation from the grid to the PV ground is absent. Hence a leakage current flows from grid to the inverter that may be hazardous if the magnitude of leakage current is beyond the acceptable limits. Also, the total harmonic distortion is another deteriorating parameter that needs to be addressed during the design of photovoltaic inverter. This paper presents state of art in the transformerless Grid-Tied inverter, includes discussion on various types of Grid-Tied inverter proposed in the literature to decrease leakage current, total harmonic distortion and the challenges that need to be addressed.

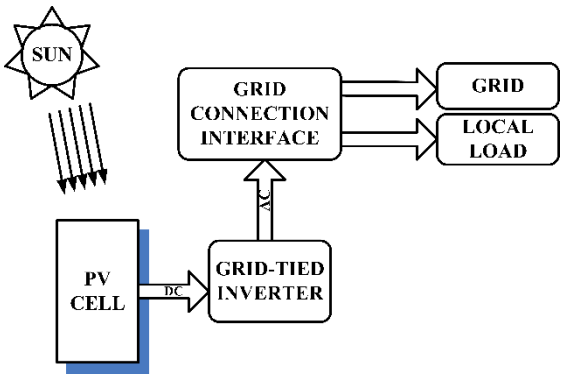


Figure 1. On-Grid System

2. Configurations and Power converters for On-Grid PV Distribution System

There are four On-Grid PV distribution system configurations available: namely Central inverter, Multi-String inverter, String inverter and Module inverter [2]. Based on power and output voltage ratings these configurations consists of PV panels or strings of PV panels, followed by DC to DC or DC to AC converters. For small residential loads, single-phase string inverters or AC or DC module converters are used. For three-phase loads, multi-string and central inverters are preferred. The various inverter topologies proposed in the literature for single-phase Grid-Tied inverters are classified as full-bridge inverters and multi-level inverters.

3. Full-Bridge Inverter

The basic structure of full-bridge inverters follows H topology and is best applicable for changing DC power to AC power. The structure of H topology is as shown in Fig. 2A. It has two legs named as leg A and B, each contains 2 power switches, & requires total four power switches. Power switches in H Bridge can be controlled by PWM technique such as Unipolar SPWM, Bipolar SPWM or Hybrid SPWM [3]. Unipolar SPWM is more preferred than Bipolar SPWM as it requires less filtering. Thus reduces the size of filter inductor required. Bipolar SPWM gives good common-mode and differential mode characteristics, whereas Unipolar SPWM has leakage current varying at switching frequency. In Hybrid SPWM two switches are gated at line frequency, hence the variation in common-mode voltage reduces to line frequency. H Bridge with Bipolar SPWM yields an efficiency of 96.5% and Unipolar SPWM, Hybrid SPWM gives 98% of efficiency. H-bridge is a simple yet efficient topology for Grid-Tied inverter. Still, to be effective an inverter must have less leakage current & high-efficiency.

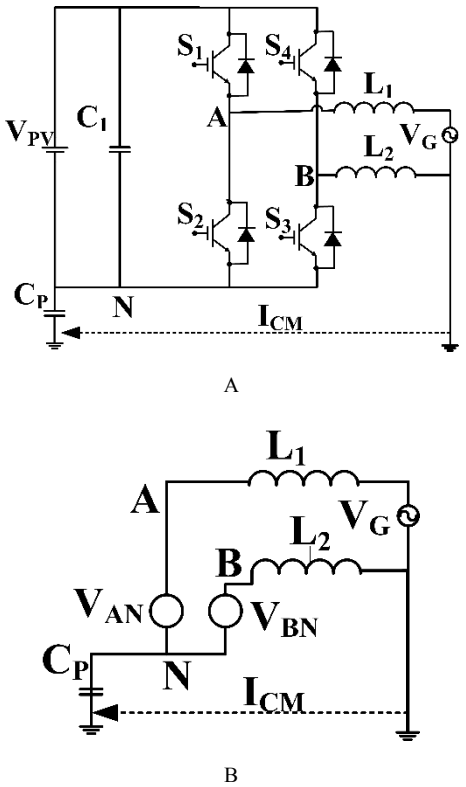


Figure 2. A. Full-Bridge Inverter B. Leakage current model

4. Common-mode Leakage Current Model

The Grid-Tied inverters are used to change the DC signal into an AC signal in the photovoltaic power generation system. To isolate inverter and the grid, a line frequency transformer is essential. The transformers of line frequency are always low-frequency transformers and therefore the inverter size and cost is usually more. The bulkiness of the inverter may lead to discomfort in the installation process and other maintenance problem. A transformerless inverter is the best solution to solve this problem. It helps to reduce PV power generation system size, costs and improves efficiency. If the transformer is removed in this process of reducing the cost and size of the inverter, galvanic isolation becomes a serious problem as it doesn't exist in the transformerless inverter. This leads to a flow of leakage current between the grid and parasitic capacitance that exists in the Solar panel. The leakage current depends on the parasitic capacitance, higher the value of parasitic capacitance more the leakage current drifts in the system. This parasitic capacitance intern depends on many elements explained in [4].

The typical value of parasitic capacitance range from 100-200pf [5]. This parasitic capacitance may vary up to 9nf if the surface is covered with water. The solar panel with the large surface may also contribute a parasitic capacitance between 50-150 nf/kW depending on the

climate condition and panel construction. The flow of leakage current in the circuit leads to several problems such as system losses, EMI and safety issues. Hence, it is required to lessen the leakage current in the Grid-Tied inverter system. According to German DIN VDE 0126-1-1 standard, it is essential to disconnect the inverter from the grid within 0.3 seconds, if the leakage current is about 30mA. Similarly, it should be disconnected within 0.04seconds if it is 100mA to keep the system safe. Fig. 2B shows a simplified common-mode leakage current model. It can be observed that the main sources of leakage currents are V_{AN}, V_{BN} and Grid (1). By analysis, it is observed that the total leakage current is given by (2), (3) [5].

$$I_{cm} = I_{cm1} + I_{cm2} + I_{cm3} \quad (1)$$

$$I_{cm} = \frac{(j V_{cm})}{-\frac{1}{4}w_{cm}L + \frac{1}{w_{cm}C_P}} \quad (2)$$

$$I_{cm} = \frac{C_p dV_{cm}}{dt} \quad (3)$$

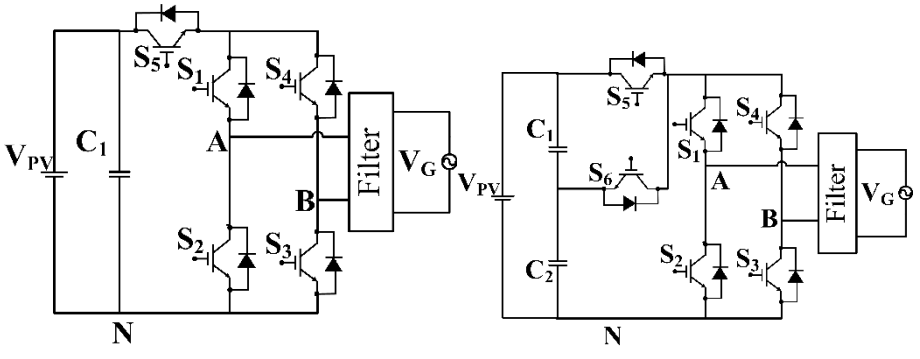
$$V_{cm} = \frac{1}{2}(V_{AN} + V_{BN}) \quad (4)$$

Where
I_{cm1} is the leakage current due to grid
I_{cm2} is the leakage current due to V_{AN} and
I_{cm3} is the leakage current due to V_{BN}

The grid frequency is very low compared to the switching rate. Hence, the main sources of leakage current can be considered as V_{AN} and V_{BN}. From (3), it can be noted that, if a common-mode voltage is kept persistent in all the commutation stages, then it is likely to keep the leakage current zero [6] [7]. The common-mode voltage in full-bridge inverter has high-frequency variation, this gives high leakage current and Electro-Magnetic Interference. So, it is essential to find a technique to maintain the common-mode voltage persistent to keep leakage current zero and give better safety to the consumers. A detailed analysis of leakage current is presented in [5–13]. Different methods of preventing leakage current are presented in the literature; all these adopt the method of i. disconnecting the DC side from the AC side of the inverter that ensures no path for the flow of leakage current ii. Clamping the common-mode voltage to $\frac{V_{PV}}{2}$, this keeps the common-mode voltage constant that intern keeps leakage current zero iii. The use of virtual ground or common ground technique [14].

5. H5 Topology

Figure 3A shows the basic structure of the H5 inverter presented in [15]. This topology uses a grid decoupling strategy by using a disconnecting switch S_5 from the PV inverter. Switches S_1 and S_4 are regulated by line frequency, S_2, S_3 and S_5 at a high-frequency. H5 inverter avoids high-frequency voltage fluctuations and is a simple low loss circuit with high-efficiency, low cost and increases the reliability. Yet, the common-mode potential depends on stray capacitance. To clamp potential to half of the PV voltage in [16], H5 inverter with an additional controllable switch and a capacitor divider to form a two-way clamping branch is added and is as shown in Fig. 3B. This topology clamps common-mode voltage to persistent level, gives good differential mode features, higher efficiency than Unipolar PWM full-bridge converter. To retain the common-mode voltage constant in H5 inverter, another novel H5 inverter is proposed in [17], it consists of five switches and a 4 diode as shown in Fig. 3C. This maintains common-mode voltage constant in all the operating modes; thus reduces the common-mode leakage current. In this inverter, the leakage current has no high-frequency components and contains only line frequency components that effectively reduces leakage current below 300mA and meets international standards VDE 0126-1-1. An improved H5-D topology is presented in [18] uses a diode clamping technique with five switches to clamp the common-mode voltage to the ground during freewheeling mode as shown in Fig. 3D. S_5 is turned off during the freewheeling period and turned on during power transmission mode. By this technique, high-frequency fluctuations in the common-mode voltage present in the H5 inverter is removed.



A B

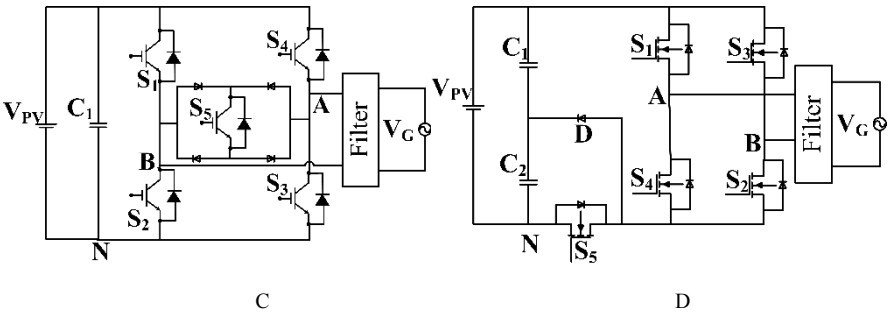
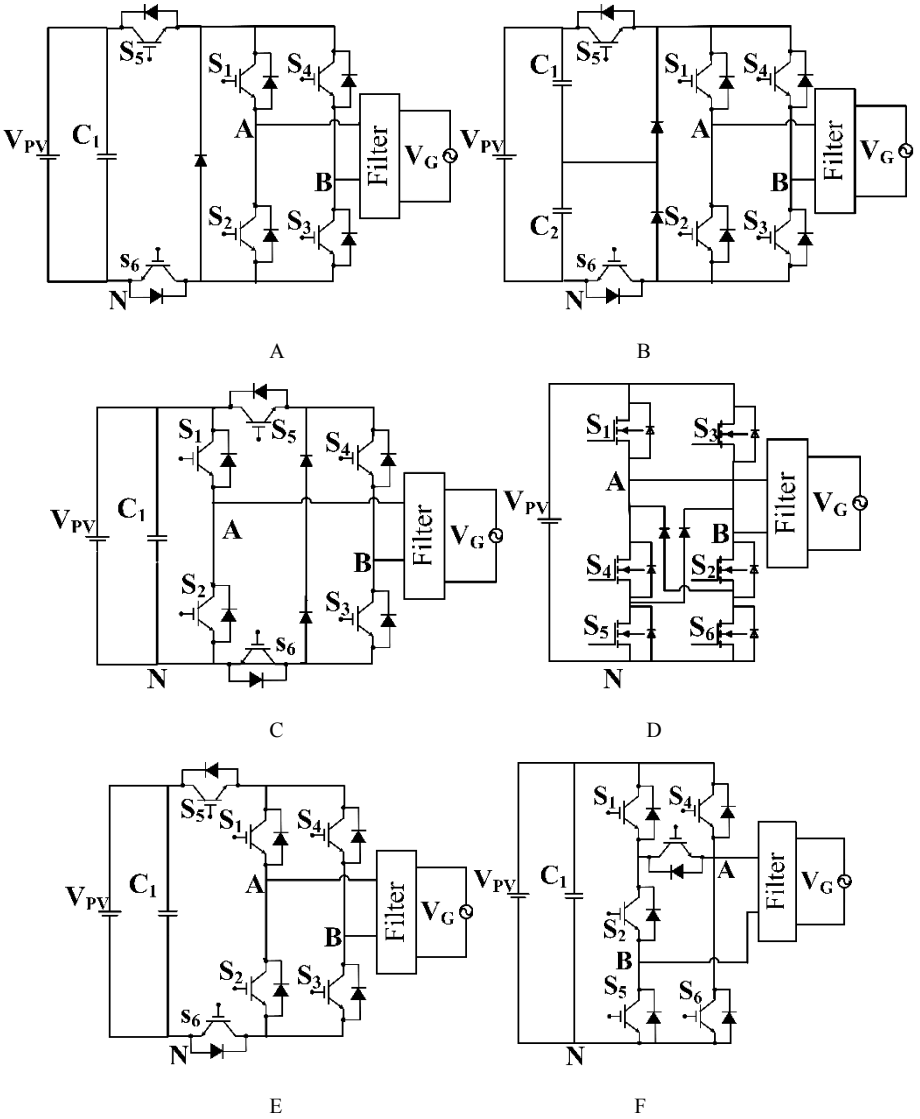


Figure 3. H5 Topologies A. H5, B. oH5, C. Novel H5, D. H5-D

6. H6 Topology

Full bridge DC bypass inverter is proposed in [19] has six switches and one diode as shown in Fig. 4A. It has a basic H bridge topology, to provide decoupling two extra switches S_5 and S_6 along with one diode D is added at the DC side of the inverter. S_5 and S_6 are controlled by a pulse width modulated signal at the high switching frequency. As both are turned ON and OFF at the same order it doesn't produce common-mode voltage. The inverter efficiency is 96.3% at the lowest input voltage. A transformerless inverter, known as H6D2 is presented in [20] is as shown in Fig. 4B. This topology with two diodes and a capacitor network limits the obstructive voltage of S_5 and S_6 to half of the PV voltage. This removes common-mode voltage. It exhibits European efficiency varying between 97.16% and 95.2% in the input voltage range of 350–800 V and can operate with any power factor. Another H6 inverter is presented in [21] that use six switches and two freewheeling diodes as shown in Fig. 4C. It works with Basic SPWM as well as Bidirectional Sine PWM. This inverter can assure no leakage current, high reliability, low total harmonic distortion (THD), high power density and high efficiency. Also, it requires input voltage same as a full-bridge inverter. Another novel, high-efficiency inverter using MOSFETs H6 type structure is presented in [22]. It is composed of six switches $S_1 - S_6$, two freewheeling diodes D_1 and D_2 and an output filter as shown in Fig. 4D. The middle switch operated at line frequency. S_1, S_6 and S_2, S_5 gated alternatively at switching frequency. This topology is suitable for non-isolated ac-module, gives European efficiency of 98.1%, smaller output inductance filter are required compared to the full-bridge Bipolar PWM scheme and low harmonic distortion. An improved H6 inverter is proposed in [23] that uses only six switches $S_1 - S_6$ and removes the leakage current is as shown in Fig. 4E. This inverter can be operated either by Unipolar SPWM or double frequency Sine PWM control strategy to give three-level output. This reduces the total harmonic distortion and hence the filter requirement. The switches work at half of the PV voltage, thus reducing switching losses and increases performance. The three-level inverter is presented in [24], uses only two extra switches in H bridge inverter as shown in Fig. 4F to keep the common-mode voltage constant. In this topology, the common-mode voltage frequency is low compared to H Bridge inverter and maintains the leakage current peak value below 300mA, and provides low total harmonic distortion. After the detailed analysis of H5 inverter, a family of new H6 topologies is presented in [25]. Here, a switch is inserted between the midpoint of one of the bridge leg and input. In the topology shown in Fig. 4G, a switch is connected between leg A and the input, and in the topology shown in Fig. 4H, the switch is connected between terminal B and input positive. These new switch connections provide an alternative current path that helps in maintaining the leakage current to lower value. When matched to H5 and HERIC inverters this topology has conduction losses more than HERIC but less than H5. The common-mode voltage is constant. It can inject or absorb reactive energy that fulfils the VDE-4105 requirement. H5, HERIC and H6 topology European efficiencies are 96.78%, 97% and 97.09%, respectively. Also, it gives excellent differential mode performance with unipolar SPWM. Fig. 4I, Shows a high-efficiency single-phase transformerless photovoltaic inverter and evaluated in [26]. It makes use of existing topology [22] and eliminates common-mode voltage and current problem in a non-insolated H6 type system. It uses a Hybrid SPWM technique, features excellent differential mode and high-efficiency. H6-N topology is proposed in [27] that include full-bridge inverter with two extra switches symmetrically employed at the DC sides as shown in Fig. 4J. This arrangement maintains the common-mode voltage steady and reduces the leakage current compared to the topology of H5 and H6 and gives low THD. Fig 4K, shows the topology of H6-type PV inverter proposed in [28] is derived from high-efficiency H6 type inverter. Here, diodes are removed and MOSFETS are replaced with IGBTs. This topology provides an excellent differential mode and common-mode characteristics by employing Unipolar SPWM. This maintains the common-mode voltage stable and can eliminate the threat of leakage current and can also feed reactive energy into the utility grid with low THD. The topology presented in [24] provides less conduction loss, however, the inverter output terminals float during the freewheeling period; hence the common-mode voltage fluctuates. A switch S_7 is included with the help of split capacitance branch as

shown in Fig. 4L proposed in [29]. It eliminates the leakage current and also can generate reactive energy. It uses a topology presented in [24], It achieves European efficiency of 97.61%. A novel active clamping circuit is shown in Fig. 4M is proposed in [30] to decrease the leakage current. The active clamping used in the topology helps in clamping the common-mode voltage during the freewheeling stage to a constant value. This topology also addresses the issue of high ripples in leakage current due to stray capacitance of switches. It reduces the conduction losses, THD, and the leakage current is found to be 11.257mA with high efficiency of 98.1%. Active clamped snubber based inverter with a DC link capacitor is proposed in [31]. The topology consists of seven switches, the effect of junction capacitors is removed by adding switch S_7 and a snubber circuit made up of two switches S_5, S_6 and a parallel snubber capacitor for the switches as shown in Fig. 4N, to keep the common-mode voltage constant, this topology decouples DC side from the AC side during the freewheeling mode. This DC link capacitor eliminates probable voltage unbalance because of two or more capacitors present in the other topologies.



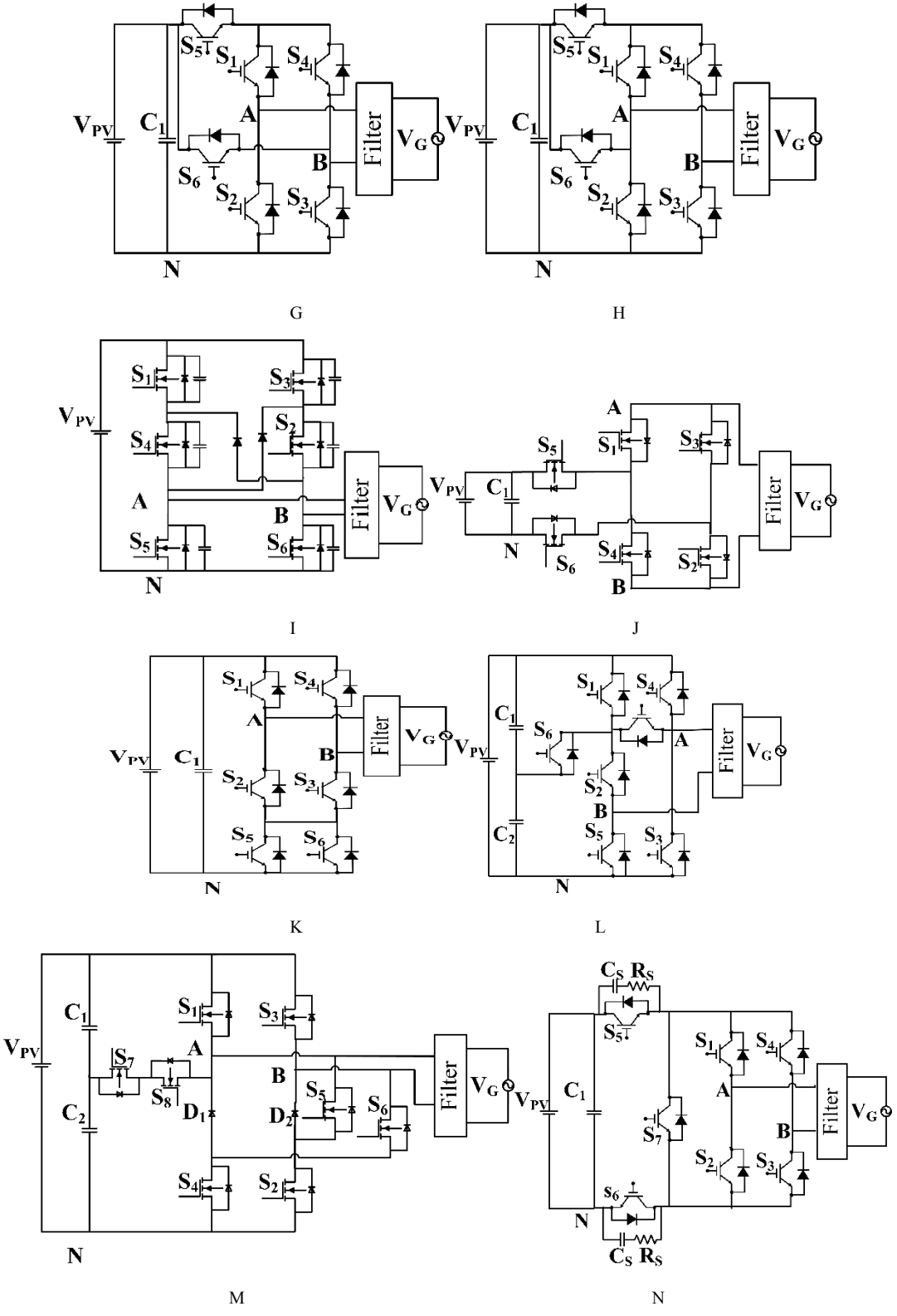
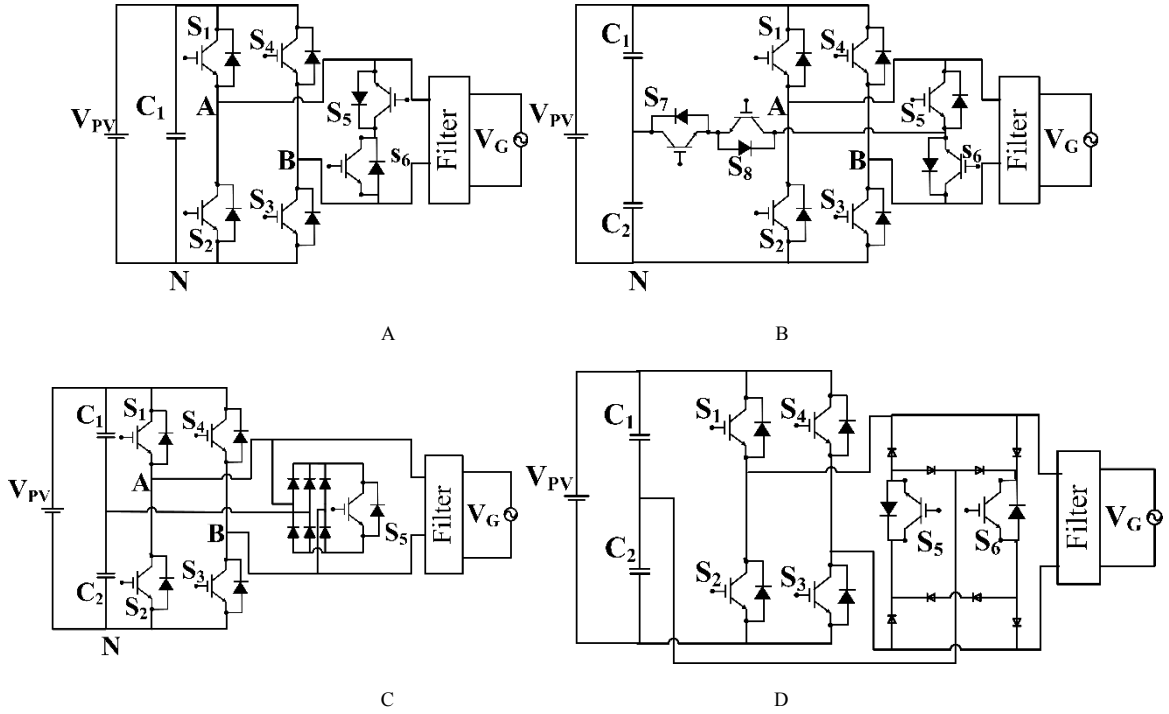


Figure 4. H6 Topology A. FBDC bypass, B. H6D2 C. Hybrid H6, D. High efficiency MOSFET H6, E. Improved H6, F. 3LH6, G. H6-A, H. H6-B, I. High Efficiency H6, J. H6-N, K. H6, L. Improved H6, M. H6-active clamping, N. H6 active clamped snubber based

7. HERIC Topology

Sunway's AG presented a Heric topology with six switches as shown in Fig. 5A [32]. It contains S_5 and S_6 disconnect switches attached to the inverter's AC side in the freewheeling mode to isolate the DC side from AC

side. This topology is controlled by unipolar SPWM. During active mode, only two switches lead to conduction losses, which improves the inverter performance. An improved Heric topology named as oHeric is proposed in [33] consists of bi-directional switch S_7 and S_8 as shown in Fig. 5B. Switch S_5 and S_6 operates for a half cycle with a low frequency and for another half cycle with a high-frequency. It can function in any power factor. The strategy used to remove leakage current is same as oH5 in which the common-mode voltage is fixed to the midpoint capacitor to maintain at half of the PV voltage. The outcome shows that oHeric leakage current is around 2.4mA which is quarter of Heric structure. Due to unideal factors such as circuit asymmetry, time of turning, or predefined dead-times, the leakage current is not eliminated in Heric topology. The resonance produced by the inductor and the junction capacitance of the switches adds high-frequency features to the leakage current. To avoid it an Enhanced Heric topology with hybrid clamping technique is introduced in [34]. This clamping network contains six diodes and a switch at the AC side as shown in Fig. 5C. Compared to traditional HERIC Inverter, the leakage current is reduced, gives good differential mode characteristics and reduces THD. Due to the effective clamping of $V_{CM,}$ the leakage current is further eliminated and is less than 15mA. The leakage current spectrum in Heric and Enhanced Heric structure shows that switching frequency and multi-switching frequency components are successfully blocked in Enhanced Heric. The hybrid clamping diode rectifier introduces some more losses. The efficiency of this topology is 97.5% at about 1kW which is very close to Heric topology and the total harmonic distortion is 2.58%. For clamping V_{CM} voltage to $V_{pv}/2$, a mid-DC-link (MDL) clamping configuration is proposed in [35] that removes leakage current by removing high-frequency components. It has a mid-DC-link clamping branch, consisting of four diodes and split capacitor, to clamp the common-mode voltage to half the DC-link voltage ($V_{PV}/2$) as shown in Fig. 5D. Such diodes regulate the voltage between A and B to the mid-DC connection voltage when the inverter is in the freewheeling mode. Thus setting V_{cm} to the desired value of $V_{PV}/2$. The leakage current in this topology is about a peak value of 25mA and RMS value of 17.7mA. AC based decoupling circuits doesn't contain clamping ability and hence inattentive high-frequency resonance further increases leakage current. A family of topology based on Heric structure is derived by using active and passive clamping technique. This gives low cost and high-efficiency inverters [36]. Four topologies are proposed, among those two uses passive clamping technique and remaining two makes use of the active clamping technique. As shown in Fig. 5E, and Fig. 5G, between the split capacitor midpoint and the bidirectional switch network, the active switch is mounted. Similarly, a passive diode-clamping branch is inserted between the midpoint of the input split capacitor and the switch network on the AC side as shown in Fig. 5F and Fig. 5H. These inverters effectively clamp the common voltage and hence eliminate dc leakage current. The grid current's THD is just 1.7% and its maximum efficiency is 97.8% and the European efficiency is 97.0%, which are very similar to that of HERIC's topology, these topologies have reactive power generation capability.



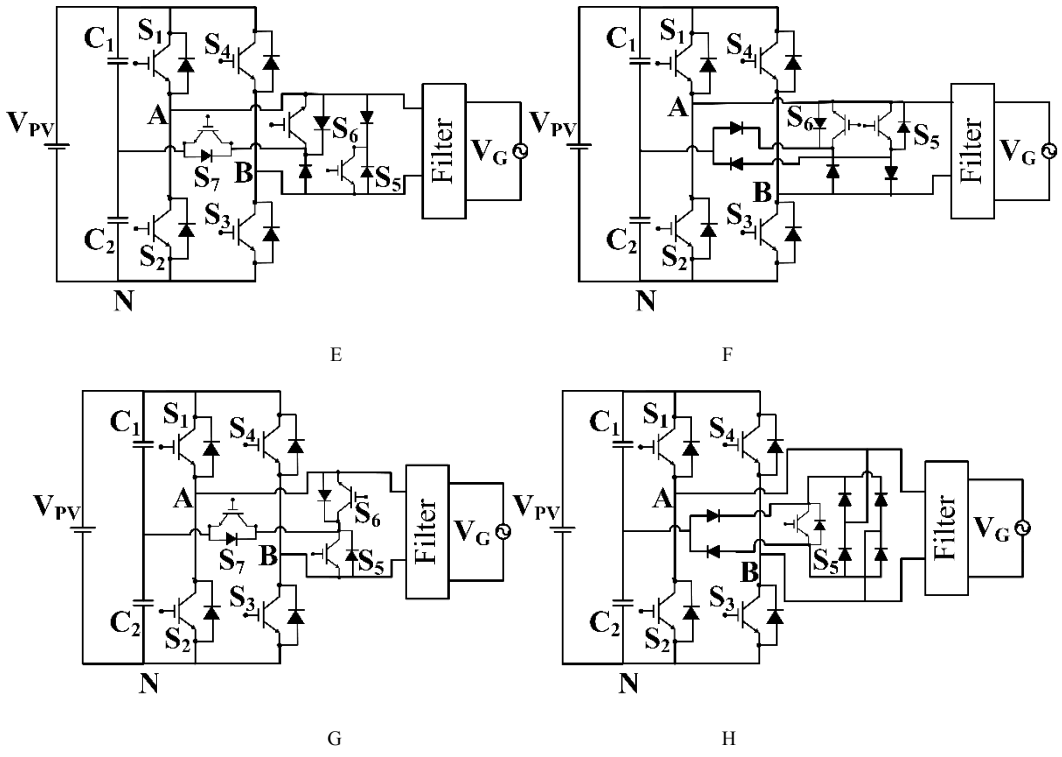


Figure 5. Heric Topology A. Heric Basic Structure, B. oHeric, C. Enhanced Heric, D. Mid-DC-link, E. Active clamping 1, F. Passive clamping 1, G. Active clamping 2, H. Passive clamping 2

8. Multilevel Inverter

It is possible to reduce the total harmonic distortion by increasing the number of voltage levels for producing step waveform that approaches the sinusoidal wave. With an increase in the number of levels, it is possible to reduce the filter requirement and hence high efficiency can be achieved. This can be attained using multilevel inverters. In a multilevel inverter, multiple voltage levels are obtained by different voltage level DC bus. Also, multilevel converters have the advantage of operating the switches at a fundamental frequency which intern reduces the switching losses present in inverters that uses high-frequency switching for the conversion. There are different types of multilevel inverters used in Grid-Tied inverter application such as half-bridge diode clamped, full-bridge single-leg clamped, cascaded (CC), Step, Magnetic Coupled, Flying Capacitor (FC) [37] etc. From the recent innovations, we can classify the multilevel inverter into diode clamped/ NPC inverter, cascaded inverter, flying capacitor /common ground inverter.

9. Neutral Point Clamped Inverter

Diode clamped/ NPC inverter is configured using a half-bridge or full-bridge [37]. Fig. 6A, Fig. 6B shows half-bridge inverter with diode clamping technique producing three levels and five-level outputs respectively. It can be observed that the number of DC input sources and the power switches increases with an increase in the number of levels. Hence, there is always a trade-off in selecting features for diode clamped inverter.

Fig. 6C, Fig. 6D shows topology of a full-bridge single-leg, switch clamped and the diode clamped inverters. The main advantage of this structure is it needs small DC bus voltage related to half-bridge. Hence, suitable for using in cascaded inverters. Fig. 6A shows a three-level NPC inverter proposed in [38]. This adds a new capacitor divider connected to the neutral grid terminal, ensures that DC will not be injected into the grid, and maintains advantages of basic clamped inverters such as no high-frequency CMV, leakage current and high efficiency found to be 98.16 in contrast with basic structure 97.1%. Families of NPC inverters are presented in [39] to remove leakage current effectively. Two basic cells are formed to insert within an existing topology like oH5 and a novel PN-NPC, NP-NPC, DP-NPC and DN-NPC structures are built. Fig. 7A shows PN-NPC Topology. It is observed that PNNPC topology has the leakage current that is same as in FB-DCBP and less than oH5. Efficiency is greater than FB-DCBP and oH5. Also, it has excellent differential mode characteristics, efficiency is better than that of oH5 and FB-DCBP, the CMV is clamped to zero, reduces leakage current and has the capability of injecting reactive power. In oH5 during

the dead time, it is found that junction capacitance of the switches forms the resonance due to non-clamping of the common-mode voltage, which gives high-frequency components in leakage current. To address this issue improved oH5 named as Improved FBNPC is proposed in [40] as shown in Fig. 7B. To reduce the effect of junction capacitance it is found that the junction capacitors of switches

$$C_4 >> C_5 + C_6 \quad (5)$$

$$C_3 >> C_5 + C_6 \quad (6)$$

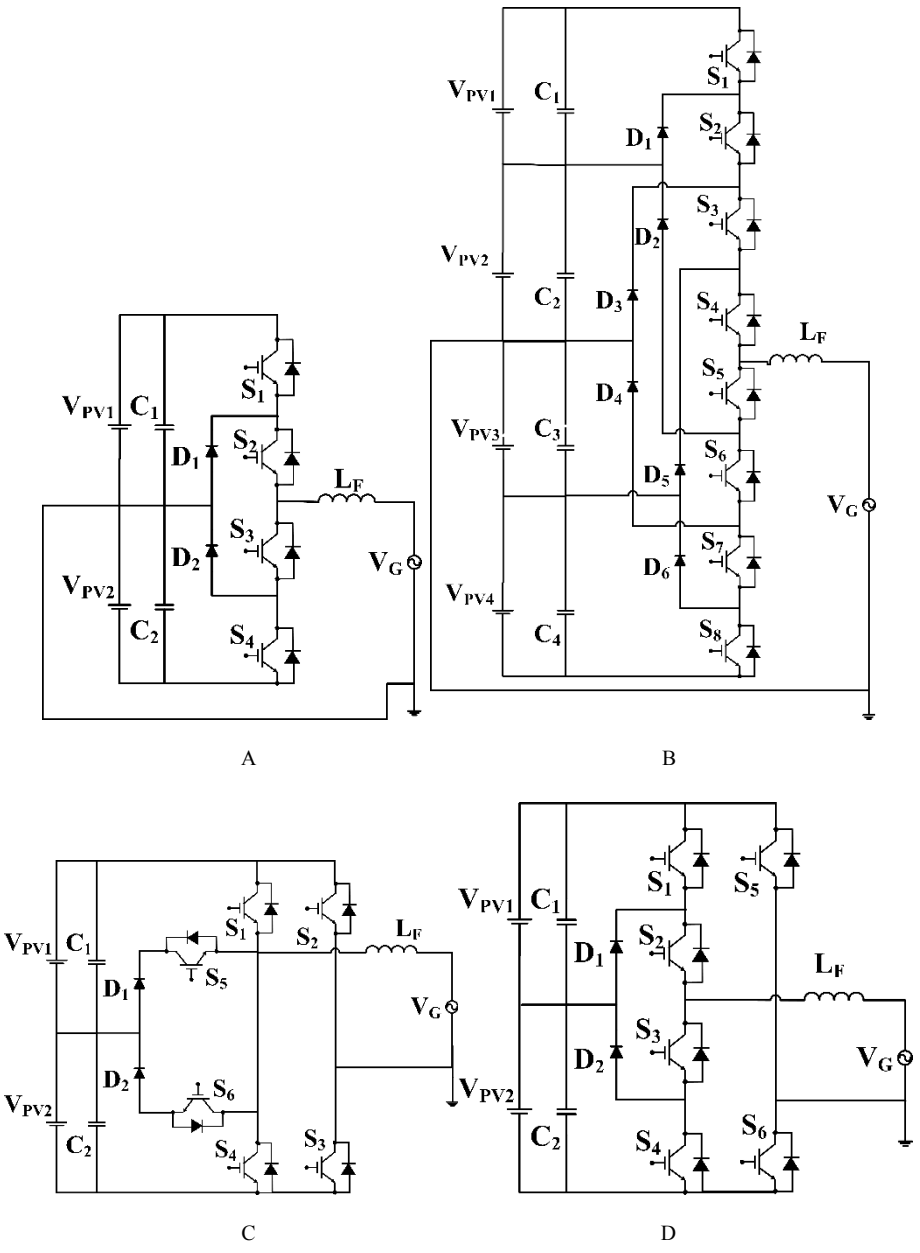
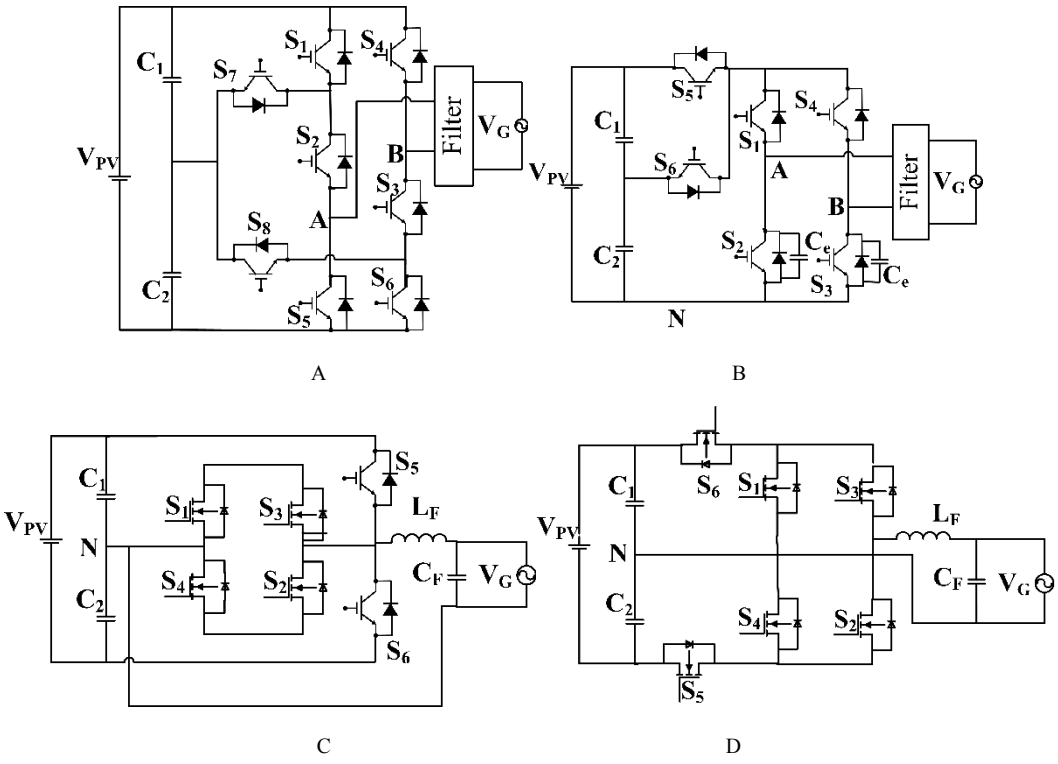


Figure 6. NPC Basic Structures A. Half Bridge Diode clamped 3 Level, B. Half Bridge Diode clamped 5 Level, C. Full Bridge single leg switch clamped, D. Full Bridge single leg

To achieve this condition, a large capacitor C_e is connected in parallel with switches. The simulation results show that this topology clamps common-mode voltage to persistent thus reduces leakage current, gives high differential mode characteristics and leakage current has less high-frequency components. Yet, due to additional capacitors, the switching losses are increased. It is found that the conduction losses in diode path are more than switches hence to eliminate the conduction path through the diode a three-level T type NPC topology is presented in [41] known as diode free T-type three-level neutral point clamped topology. The topology structure is as shown in Fig. 7C. This has no diodes involved in the current path and hence provides zero vector loss. Active neutral point clamping is studied and analyzed in [42] to propose a new ANPC structure as shown in Fig. 7D that uses MOSFETs bidirectional conduction capability throughout the freewheeling stages. To maintain high efficiency under different conditions like different load, heat sink temperature and different frequencies SiC MOSFETs are used in this inverter. As SiC MOSFETs have small dead time the shoot-through problem can be reduced. The shoot-through problem occurs in the inverter when all the switches are ON and starts conducting, this increases the current flow in the inverter. To avoid this effect, a dead time is provided between switching states. A novel three-level NPC inverter is proposed in [43] that use only four switches and two diodes as shown in Fig. 7E. This topology reduces the leakage current as it uses a Neutral point clamping. Also, it avoids the effect of the shoot-through problem without adding dead time, here the NPC circuit and the filters are separated by the bridge leg to remove shoot-through. Compared to NPC half-bridge and dual buck half-bridge converters, it has a less conductive loss. In oH5 due to junction capacitance, the leakage current is more. A NIFB-NPCI [44] topology proposed as shown in Fig. 7F reduces the leakage current due to unideal process parameters at switching frequency. It locks the CMV oscillations to constant thereby limits the leakage current at switching frequency, without dead time. Another NIIFBC is presented in [45] that uses super-junction MOSFET as shown in Fig. 7G. This inverter reduces the shoot-through and thus increases the inverter's performance. Further, the clamping branch with two switches ensures low leakage current by CMV clamping technique. Gives an efficiency of 98.3% and 98.8% of high European and peak efficiencies respectively. It has low leakage current and good differential mode characteristics. An M-NPC topology is presented in [46] using SJ-MOSFET for achieving high efficiency. In this CMV is completely clamped to half of the PV voltage with the clamping branch. SJ-MOSFET neutral point clamped inverter with seven switches and a four diode is as shown in Fig. 7H. This has a full-bridge configuration with common-mode voltage clamping network that offers a freewheeling pathway for the flow of leakage current through the diode. This M-NPC topology is presented by substituting the IGBTs of PNNPC inverter to gain the advantage of PNNPC for eliminating leakage current and MOSFET for obtaining high efficiency.



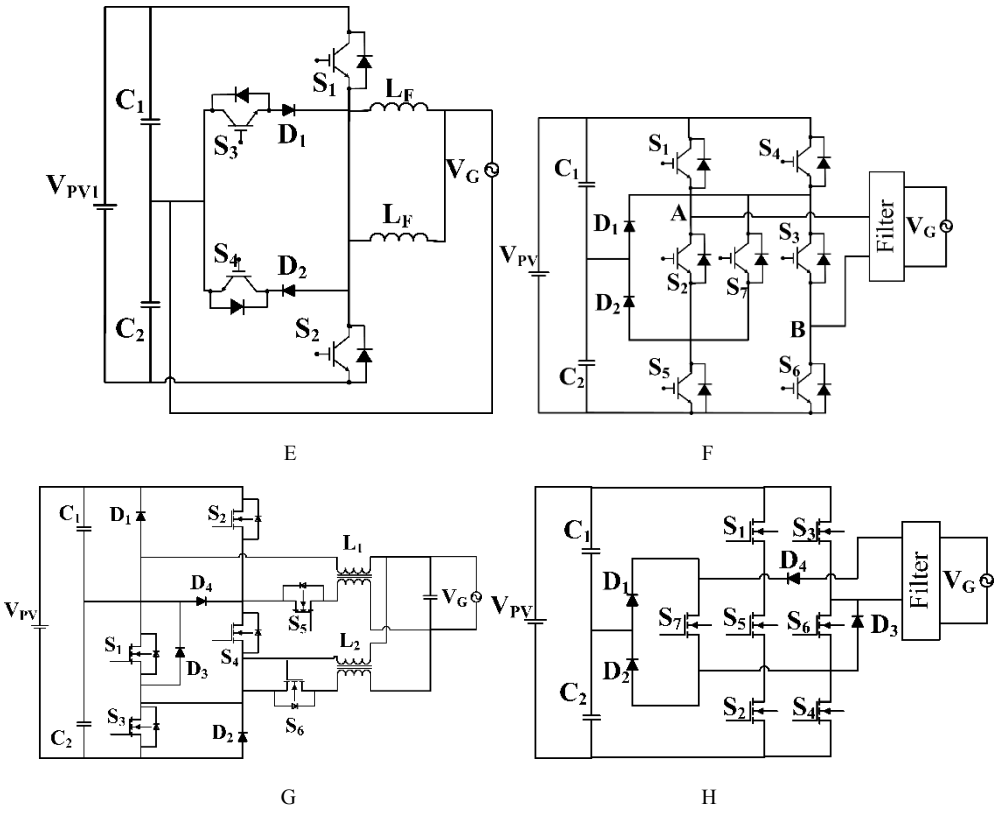
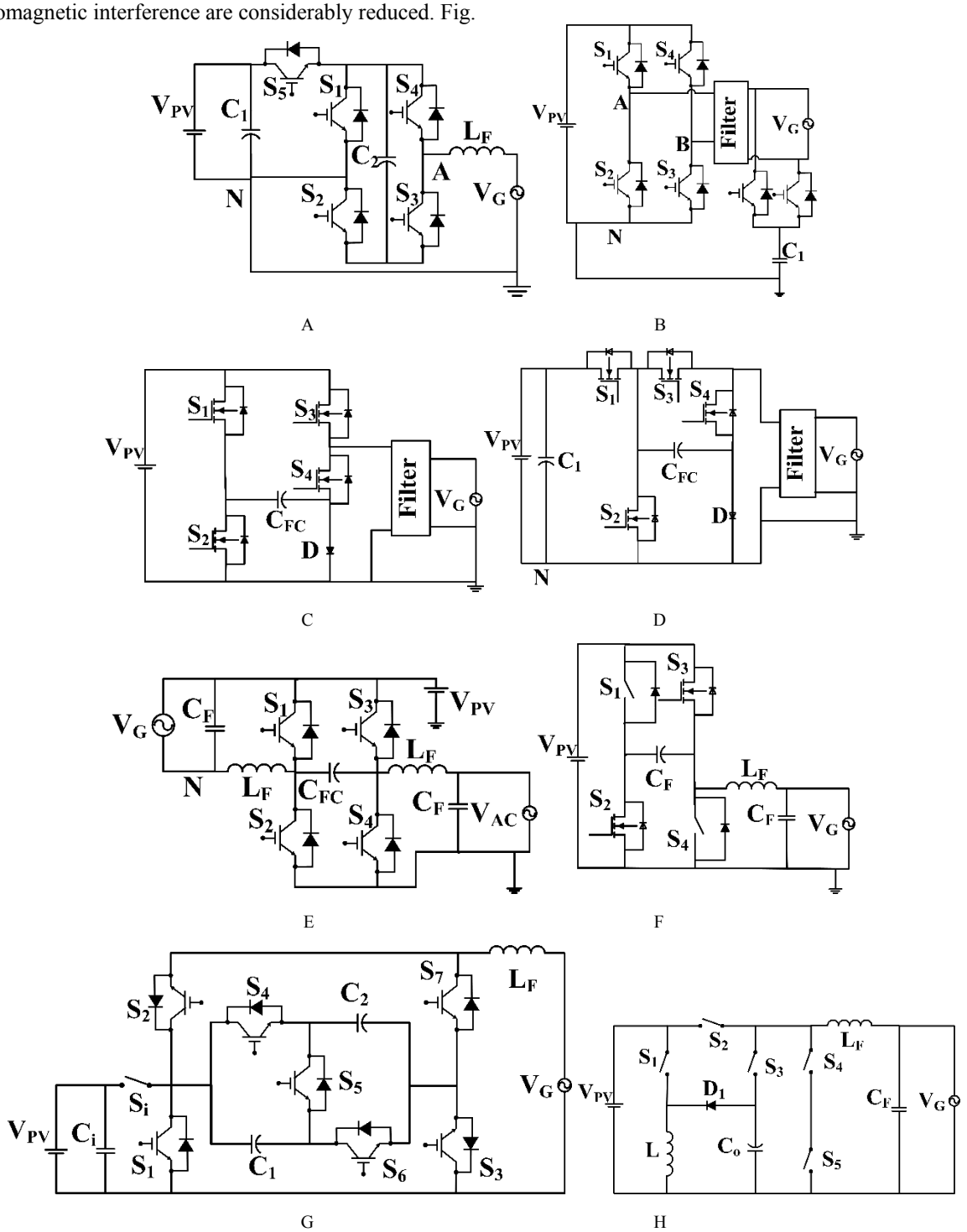


Figure 7. NPC Topologies A. PNNPC, B. Improved FBNPC, C. T-Type 3L, D. ANPC, E. HBNPC, F. NIFB-NPCI, G. NIIFBC, H. MNPC

10. Common Ground Type Inverter

In the virtual bus concept of reducing leakage current, the PV negative terminal is linked to grid ground point to make the CMV zero. Hence the output voltage in this kind of topology is either zero or positive. To get a negative voltage virtual ground must be formed while designing the topology. In virtual ground technique, the leakage current is eliminated naturally. [47] Proposes one such novel inverter that uses a virtual DC bus concept as shown in Fig. 8A. It makes use of five switches, single filter and is appropriate for small power uses. An AVG i.e. active virtual ground topology is presented in [48]. This inverter includes two power switches and capacitor in the AVG network as shown in Fig. 8B. This network makes sure that the high-frequency current component doesn't flow to the input from the ground. Hence decreases the leakage current. The foremost advantage of this inverter is it gives low high-frequency leakage current, unipolar switching reduces the filter requirement, combination of MOSFET and IGBT can be used to reduce the switching losses. [49] Presents a group of flying capacitor topologies based on the virtual ground or common ground concept. It introduces three topologies named as Type I, Type II and Type III as shown in Fig. 8C, Fig. 8D, Fig. 8E, respectively. It has reactive power compensation ability. The maximum output voltage is V_{PV} unlike in NPC where the peak is half of the V_{PV} voltage. In [50] a flying capacitor type common ground inverter topology is presented as shown in Fig. 8F. The flying capacitor helps in generating the negative voltage. This topology has only one device in the current pathway during all modes. Hence this improves the overall efficiency of the inverter. [51] Presents five-level boost topology as shown in Fig. 8G. This topology achieves an efficiency of 96%. A common ground topology with 5 switches and one diode is proposed in [52] is as shown in Fig. 8H, the capacitor charges with a dedicated switch that reduces the size of the capacitor. It works with sine PWM, offers minimal leakage current, requires small filter due to SPWM, and provides low switching losses, low EMI and low ripple in the output current. Also during active mode current flows through only one device hence reduces the conduction losses. Fig. 8I shows a five-level inverter proposed in [53] that uses common ground configuration. The flying capacitor helps in generating multilevel output in this topology, and hence reduces the filter requirement and also harmonic. The common ground ensures less leakage current. The usual PWM modulation can be used for switching the devices. The five levels of output reduce the overall harmonic distortion and hence it gives a good performance. A novel nine-level topology is proposed in [54]. This comprises of two full cascaded bridges with various link voltages as shown in Fig. 8J. One bridge is connected to a single DC bus and other bridge is fed from the flying capacitor. It also proposes an appropriate switching scheme to control the flying capacitor which minimizes the common-mode leakage current and

improves the efficiency. To preserve a small leakage current, switches with very low voltage drop, like MOSFETs are used in one of the two legs. The other leg uses IGBTs with fast antiparallel diodes, where high-frequency hard switching commutations occur. Due to nine levels at the output, harmonic distortion and electromagnetic interference are considerably reduced. Fig. 8K shows another common ground topology in this a negative voltage is generated by switching ON the power device S_4 that charges the capacitor C_2 [55]. This topology uses a minimum number of components, hence its design cost is low. Also, it is likely to achieve higher power density & maximum efficiency of the topology is 97.4%.



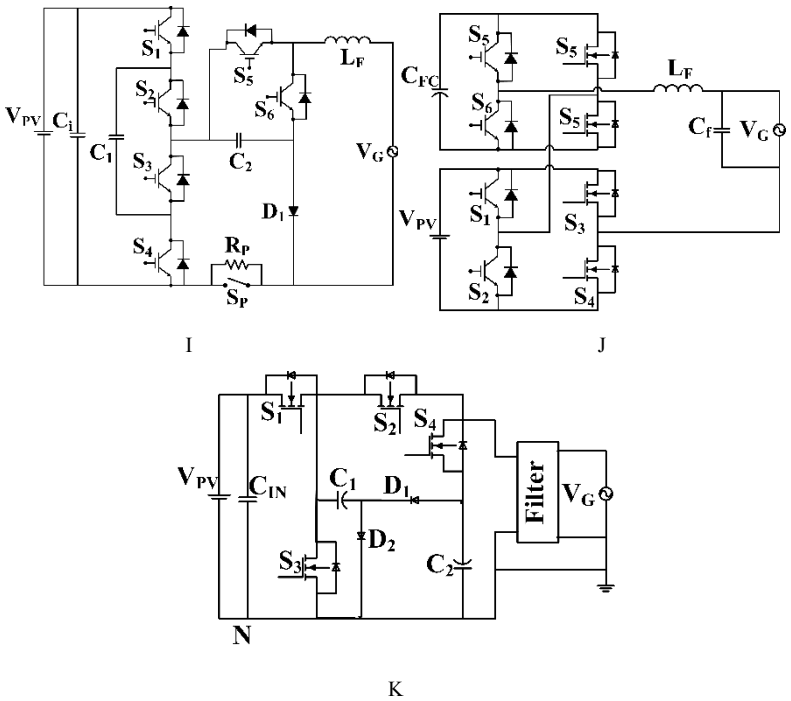


Figure 8. Virtual Ground / Common Ground (CG) A. Inverter with Virtual DC Bus, B. AVG, C. Type I, D. Type II, E. Type III, F. Flying Capacitor, G. CG 5L, H. CG, I. Multilevel CG, J. 9L CFB, K. CG

11. Comparison of Grid-Tied Inverter

The various parameters that need to be considered while designing inverter are Efficiency, Harmonic distortion, Islanding, Interruption of line connection under load, sensitivity to control signal on the line, Electromagnetic capability, MPPT. And the other common parameters are leakage current, common-mode voltage. From the above discussion, we can summarize that in full-bridge or H bridge inverters DC decoupling/AC Decoupling and/or clamping technique is used to reduce the leakage current. In DC decoupling as current flows through the switches during active mode the losses are increased [56]. In AC decoupling the leakage current flows through only the cell created for decoupling the inverter from the AC side of the circuit. Yet high-frequency variation may occur in leakage current that can be considerably reduced using active or passive clamping branch. In inverters that use clamping branches, requires split capacitors. These spilt capacitors must be balanced perfectly to achieve the goal of maintaining common-mode voltage constant, else again it will add up the leakage current. Also, it is found that the NPC topology requires double the input voltage required compared to full-bridge topologies.

Table. 1. gives the comparison of various On-Grid inverters discussed in the paper. It also summarizes the features and critical findings of these topologies. It is observed that the efficiency of common ground topology is about 99% which is very high compared to other techniques used to eliminate leakage current. In common mode topology, large capacitors are used to hold the charge for the generation of the negative cycle.

It can be witnessed that most of the inverters proposed have leakage current that meets the standards. Yet, only a few topologies have addressed the other causes of leakage current variation at switching frequency. Hence, it is required to do the analysis of resonance caused by parasitic capacitance and the filter network. Generally, the effect of it is rarely considered as it is assumed to be very low, but the junction capacitance may vary from several pf to nf, this may cause high-frequency variation in leakage current due to the resonance. Hence, it is important to analyze the effect of junction capacitance in the present inverter topology.

Shoot-through is another problem that may lead to serious issues. It occurs when all the switches are turned ON. Even though in the modulation technique ideally all the switches are not turned ON, but in the practical situation due to various delays and the other issues there may be a chance that all switches will be ON sometimes for a small period. During this situation, a high current starts flowing through the circuit that will damage the inverter. A dead time introduced in the modulation techniques to avoid this problem, using SiC MOSFET switches in place of IGBT and MOSFET is another solution to solve this issue as it has low switching time. Further, its effect needs to be analyzed in the existing topologies to find other suitable technique that can be introduced in the existing topologies for improving the performance and reliability. Hence it is better to analyze the effect of junction capacitance as well as shoot-through while designing the inverter along with other parameters.

Table 1. Comparison of Grid-Tied Inverters

Reference	S	D	Cin	fsw	Vg/ fg	VPV	Lf	Cf	Vomax	P	Icm	THD	η	Features	Findings
H5 [15]	5	5	1	16	NA/50	NA	NA	NA	VPV	NA	2.8 [16]	NA	NA	A decoupling switch used	• Avoids high-frequency voltage fluctuations • Simple low loss circuit with high-efficiency, low cost • Increases the reliability
oH5 [16]	6	6	2	20	240/50	340-700	4 (2)	6,6	VPV	1	1	NA	NA	Freewheeling path clamped to VPV/2 with a bidirectional switch	• Good differential mode characteristics, • Higher efficiency, losses are less compared H5
Novel H5 [17]	5	9	1	10	220/50	400	5 (2)	NA	VPV	1.5	<30rms	<5	NA	A single switch and 4 diodes are used for decoupling network.	• Reduces common-mode leakage current. • Leakage current has no high-frequency components and contains only line frequency components
H5-D [18]	5	6	2	20	220/50	380	1 (2)	NA	VPV	0.63	120p-p	4.88	>H5	A diode introduced to reduce the effect of junction capacitance.	• Common mode voltage remains constant • High-frequency fluctuations in leakage current reduced
FBDC [19]	6	7	1	16	NA	350-800	1.5 (2)	NA	VPV	5	NA	NA	96.3	Two extra switches and a diode is used in decoupling network	• Common mode voltage remains constant • Theoretically leakage current is zero
H6D2 [20]	6	8	2	16	230/50	350 - 800	3 (2)	NA	VPV	5	0.7 [16]	NA	97.4	A split capacitor network with extra 2 switches and 2 diodes are used.	• No varying common-mode voltage • Requires low-input voltage • Can operate with any power factor.
Hybrid H6 [21]	6	8	1	16	220/50	350	5 (2)	NA	VPV	1	<30	2.8	96.7	Uses 6 switches and two freewheeling diodes	• It can guarantee no leakage current, • High reliability, power density and efficiency • Low THD • It requires input voltage same as a full-bridge inverter.
High-efficiency MOSFET H6 [22]	6	8	NA	30	120	180-200	1.6, 0.5	0.68	VPV	0.3	NA	NA	98.1	MOSFETs are used for all the switches This circuit is suited for non-isolated ac-module	• It gives high efficiency over wide load range • Low ground leakage current, THD

Table 1 Continued

Improved H6 [23]	6	6	1	20	220/50	380	4	NA	VPV	1	≈0	2.543	97.1	It has 6 switches that includes 2 decoupling switches	• less filtering is required • Low Switching losses, low THD • Effect of junction capacitance is analyzed and addressed
3L H6 [24]	6	6	1	10	220/50	400	2 (2)	9.4	VPV	3	<300p	NA	NA	Has two asymmetrical distributed switch	• Keeps the common mode voltage constant. • Provides low THD.
H6-A, B [25]	6	6	1	20	230/50	380-700	3 (2)	0.47	VPV	1	9	NA	97.09	Derived from H5, hybrid H6, and Heric topologies New switch connections provide an alternative current path during the freewheeling mode.	• Conduction loss greater than Heric less than H5 • Has the capability of injecting or absorbing reactive power. • Common mode voltage is constant • Gives excellent Differential Mode performance with Unipolar SPWM.
High Efficiency H6 [26]	6	8	NA	16	220/50	400	0.88 (2)	4.7	VPV	2.2	NA	1.8	98.5	Derived from high efficiency MOSFET inverter with different freewheeling current path. Reactive power compensation is presented	• Features steady-state characteristics excellent differential mode characteristics, & high-efficiency
H6-N [27]	6	6	1	10	NA	400	1 (2)	2.2	VPV	NA	Small	NA	NA	2 extra switches symmetrically employed at the dc sides of the inverter.	• Eliminates leakage current. • Low THD. • Shoot through problem addressed • Effect of junction capacitance analyzed
H6 [28]	6	8	1	20	230/50	400	3 (2)	2.2	VPV	1	19.6rms	1.7	97.22	In high efficiency, H6 inverter diodes are removed and MOSFET's are replaced with IGBT to improve reactive power handling capability	• Provides excellent differential mode and common mode characteristics • Has the capability to inject reactive power into the utility grid with low THD.
Improved H6 [29]	7	7	2	10	230/50	400	3	0.006	VPV	3	8.1rms	1.9	97.61	An extra switch is added to decrease leakage current fluctuations	• Eliminates leakage current by CMV clamping • Has reactive power generation capability. • Independent of junction capacitance

Table 1 Continued

H6-active clamping [30]	8	10	2	40	110/50	200	1.1 (2)	1	VPV	0.3	11.257 rms	0.39	98.1	Uses an active clamping technique	• Junction capacitance is addressed. • It reduces the conduction losses, THD. • High efficiency of 98.1%.
Active clamped snubber based [31]	7	7	1	10	50	200	3, 6	0.022	VPV	1	NA	NA	NA	Active clamped snubber with a single DC link capacitor is used	• Keeps common-mode voltage constant • Effect of junction capacitor is addressed
Heric [32]	6	6	1	NA	NA	NA	NA	NA	NA	NA	5.6[7]	NA	NA	Has two decoupling switches at the AC side of the inverter	• Only two switches conduct during active mode, conduction losses reduced • Improves the efficiency
oHeric [33]	8	8	2	15	200/50	400	NA	NA	NA	5	2.4	NA	NA	Consists of bi-directional switches Adopts technique used in oH5	• Work in any power factor. • Leakage current is reduced.
Enhanced Heric [34]	5	10	2	16	220/50	400	0.8 (2)	NA	VPV	2	15 rms	2.58	97.5	Junction capacitance is addressed using hybrid clamping technique.	• Switching frequency and multi switching frequency components in leakage current effectively suppressed • Good differential mode characteristics and • Reduces THD.
Heric-MDL [35]	6	14	2	10	230/50	400	0.25 (4)	20	VPV	10	17.7 rms	NA	97.76	Uses either Passive clamping or active clamping techniques	• Effectively clamps the common-mode voltage • Eliminate dc leakage current. • The THD of the grid current is only 1.7% • Highest efficiency is very close to that of the world-leading HERIC topology. • Have reactive power generation capability.
Active clamping 2 [36]	7	7	2	16	220/50	400	0.85 (2)	NA	VPV /2	2	10	1.7	97	Based on Heric Structure topologies are derived by using active and passive clamping technique	• gives low cost inverter • high efficiency

Table 1 Continued

PN-NPC [39]	8	8	2	20	230/50	380-700	3 (2)	0.47	VPV	1	3	NA	97.2	A two basic switching cells are formed to insert within an existing topologies like oH5 and a novel PN-NPC, NP-NPC, DP-NPC and DN-NPC structures are built.	• Efficiency is greater than FB-DCB and oH5. • It has excellent differential mode characteristics, • Common mode voltage is clamped to zero • Reduces the leakage current • Has the capability of injecting reactive power.
Improved FBNPC [40]	6	6	2	20	230/50	380	3 (2)	5	VPV	1	<10	NA	NA	To reduce the effect of junction capacitance a large capacitor Ce is connected in parallel with switches.	• Clamps common-mode voltage to constant • Reduces the leakage current • Gives high differential mode characteristics
T-Type 3L [41]	4	4	2	12	220	700	0.8, 0.15	10	VPV /2	5	NA	NA	#	Conduction through diode is eliminated as losses are more in diode	• Provides zero vector loss.
ANPC [42]	6	6	2	80	230/50	700	1.5	5µ	VPV /2	1.66	NA	<5%	96.43	Uses SiC MOSFETs	• Reduces the leakage current • It avoids the effect of the shoot-through problem without adding dead time, • Reduced filter requirement, THD also reduced. • Has lower conduction losses
HBNPC [43]	4	6	2	10	110/50	400	2 (2)	NA	VPV /2	1	NA	NA	NA	Leakage current due to Junction capacitance in oH5 is addressed	• Clamps the common-mode voltage to constant • Limits the leakage current at switching frequency, without dead time.
NIFB-NPCI [44]	7	9	2	20	220/50	340-700	3 (2)	2	VPV	1	3	NA	96.5	It is non-isolated type inverter	• Reduces high frequency fluctuations in leakage current • It locks the CMV oscillations to constant

Table 1 Continued

VNIIFBC [45]	6	9	2	20	220/50	400	1.5 (2)	2	VPV	1	7.6	NA	98.3	NIIFBC that uses super-junction MOSFET	• Reduces the possibility of shoot through • Improves the reliability of the inverter. • Low leakage current by clamping the common-mode voltage to constant. • Good differential mode characteristics.
M-NPC [46]	7	11	2	10	230/50	400	3 (2)	4	VPV	1	13.27	1.6	97.65	In PNNPC IGBTs are replaced with SJ-MOSFET used for achieving high efficiency.	• PNNPC eliminates the leakage current • MOSFET gives high efficiency. • Common mode voltage is constant
Virtual DC bus [47]	5	5	1	20	220/50	400	8, 0.8	0.34	VPV	0.5	10	2.1	NA	Uses virtual DC bus	• Only five power switches • Suitable for small power single-phase applications.
AVG [48]	6	6	NA	20	220	400	0.5 (2)	2.3	VPV	1	NA	NA	NA	Includes 2 power switches and capacitor in AVG network.	• Low high-frequency leakage current, • Unipolar switching reduces the filter requirement, • Combination of MOSFET and IGBT can be used to reduce the switching losses.
Type I [49]	4	1	1	20	230/50	400	0.35	2.2	VPV	1	~0	NA	99.2	Family of novel flying capacitor transformerless inverters based on the common ground concept	• Due to virtual ground, there is no leakage current • It has reactive power compensation capability • The output ac peak voltage is equal to VPV
Type II [49]	4	1	1	20	230/50	400	0.35	2.2	VPV	1	~0	NA	99.25		
Type III [49]	4	0	1	16	230/50	400	0.8	10	VPV	1	~0	NA	97.8		
Flying Capacitor [50]	4	2	NA	18	230/50	162	0.42	2.2	VPV	1	NA	<2.3	98	Flying capacitor type common ground inverter topology The flying capacitor helps in generating the negative voltage.	• One switch in the load current path during all modes of operation. • Improves the overall efficiency of the system.
CG 5L [51]	8	8	1	20	240/60	200	0.37	2.4	VPV	0.973	NA	NA	96	Five-level boost inverter with common ground connection	• Low leakage current, low THD • High efficiency

Table 1 Continued

CG [52]	5	1	NA	20	240/50	340-380	0.37	2.4	VPV	1	NA	<2	91.6	A common ground topology with 5 switches and one diode	• Requires small filter due to SPWM • Provides low switching losses, • Low leakage current EMI and THD • During active mode current flows through only one device hence reduces the conduction losses
Multilevel CG [53]	6	7	1	12	220/60	350	2	NA	VPV	1.2	~0	3.5	95.88	The flying capacitor helps in generating multilevel output in this topology	• Less leakage current, THD.
9L CFB [54]	8	8	NA	20	230/50	300	1.5	1	VPV	1	30	2.7 to 3.3	98	Two cascaded full bridges with different dc-link voltages	• Minimizes the common-mode leakage current, THD and EMI • Improved efficiency.
CG [55]	2	2	1	24	220/50	400	4	2.2	VPV	0.5	NA	NA	97.4	Common ground topology uses less number of switches	• This topology uses the minimum number of components • Design cost is low • Possible to achieve higher power density. • Good efficiency

- S number of Switches
- D number of Diodes
- Cin input capacitors / Split capacitor in µf
- Vg/fg Grid Voltage in Volts and Grid frequency in Hz
- VPV DC input voltage in Volts
- Lf Filter inductors in mH
- Cf Filter capacitor µf
- Vomax maximum output voltage
- P Power in kW
- Icm Common-mode leakage current in mA
- THD Total harmonic distortion in %
- # proposed is better than the reference

12. Conclusions

This paper presents recent trends and challenges in various H-bridge type and multilevel inverter. A comparison of the leakage current, the common-mode voltage and efficiency are done. It is noticed that further analysis of stray capacitance to reduce leakage current and shoot-through effect to avoid accidental high current flow must be considered and revisited to provide better safety that may avoid damage to the inverter. It is also required to consider an inverter topology that gives less leakage current, low THD, high efficiency under different conditions with less number of switches to decrease the total price of the inverter. And it is found that common ground technology could be a promising solution for the design of inverter as it requires less number of switches gives high efficiency due to a reduction in the conduction losses. And leakage current is zero as the common-mode voltage is zero in this type of inverter.

Nomenclature

AC	Alternate current
ANPC	Active neutral point clamping
CG	Common ground
CMV	Common mode voltage
DC	Direct current
EMI	Electromagnetic interference
FB	Full-bridge
FBDC	Full-bridge with DC bypass
HB	Half-bridge
IGBT	Insolated gate bipolar junction transistor
MDL	Mid-DC-Link
MNPC	MOSFET Neutral point clamping
MOSFET	Metal oxide semiconductor field-effect transistor
NIFB	Non-isolated full-bridge
NPC	Neutral point clamping
PV	Photovoltaic
PWM	pulse width modulation
SiC	Silicon carbide
SJ	Super junction
SPWM	Sinusoidal pulse width modulation
THD	Total harmonic distortion

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