

# Nonvolatile Memory Cell Based on Memristor

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**Abstract** Memristor, one of the fundamental circuit elements, has promising applications in non-volatile memory and storage technology as it can theoretically achieve infinite states. Information can be stored independently in these states and retrieved whenever required. In this paper, we have proposed a non volatile memory cell based on memristor emulator. The circuit is able to perform read and write operations. In this memristor based memroy cell, unipolar pulse is used for writing and bipolar pulse is used for reading. Unlike other earlier designs, the circuit does not need external read/write enable switches to switch between read and write operations; the switching is achieved by the zero average bipolar read pulse given after the completion of write cycle. In our proposed memristor based memory cell, single bit can be read and any voltages from 0 to 5 volts can be written. Mathematical analysis and the simulation results of memristor emulator based read write circuit have been presented to confirm its operation.

**Keywords** Memristor, Memristor Emulator, Memristor Memory Cell, Memristor Read, Memristor Write

## 1 Introduction

Memristor was first postulated by Leon Chua in 1971 as a fundamental circuit element [1]. In a memristor when the current flows in one direction, it's resistance decreases and vice versa. When the current flow is stopped, memristor retains its final state. This state retention property of memristor makes it useful as a non-volatile memory element [2, 3]. Important application areas of the proposed non-volatile memory cell are in next generation memory devices for use in artificial intelligence and neuromorphic computing.

Memristor is a natural application for resistive random access memory (ReRAM) technology [4]; moreover, neuromorphic computation using ReRAM technology is also becoming popular [2, 5–9]. By controlling programming signal width and/or amplitude, memristor can be taken to any state; how-

ever, two states: high resistance state (HRS) and low resistance state (LRS) are commonly used and they represent bit 1 and bit 0 respectively [2, 10–12].

Several research groups have proposed memristor emulators [13–17]. Lopez *et al.* [14] and Yu *et al.* [17] have proposed a floating memristor emulator circuit based on current conveyors. The emulator proposed by Kim *et al.* [13] is built from off-the-shelf solid state components. In this paper, [13] has been chosen for emulating a memristor because it has shown promising results that provides an alternative solution of *hp* TiO<sub>2</sub> memristor model in real circuit. Memristor memory cell architecture based on the memristor model has been proposed by [11, 12, 18, 19]. Mohammad *et al.* [18] have explored various aspects of memristor modeling and designed a memristor based memory. Likewise, Sarwar *et al.* [19] has designed memristor based nonvolatile random access memory, but the memristor in their work uses Spice model. The design analysis of nonvolatile memristor memories, [11], has been used for designing a read write circuit in this paper because their analysis have specifically targeted key electrical memristor characteristics relevant to memory operations.

Even though many researchers have proposed memristor emulator circuit and memory cell based on memristor model, *no memristor emulator based read write circuit is available*, which can correctly estimate the behavior of a real physical memristor memory cell. In [11], memristor linear model is used for realizing a memory element. In this paper memristor emulator is used for realizing a memory cell. Furthermore, the need for external read write enable switch in [11] and [12] is eliminated. Typical read/write circuit proposed in [11] is shown in Figure 1.

The unipolar write pulse and bipolar read pulse with re-defined read circuit helps to eliminate the read write enable switch. This not only completely removes switching loss in read write enable switch but also reduces the access time. Use of unipolar and bipolar pulses for reading and writing operations respectively could provide efficient architecture for the implementation of memristor-based memory.

Due to read cycle distortion, the memristor internal state may change and enter into the invalid state. This read distortion issue of the memristor memory is also investigated. Read ac-

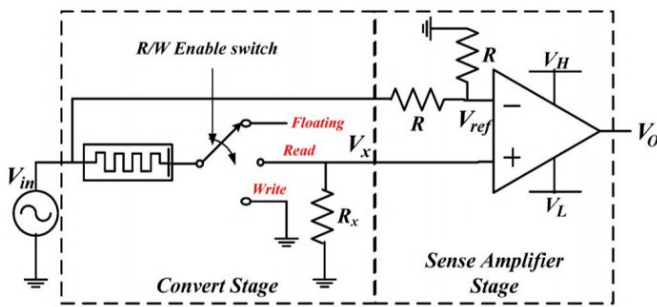


Figure 1. Typical Read/Write Circuit Proposed in [11].

cess time duration in read pattern is proposed to preserve data integrity during the read operation.

In this paper, we have used one of the basic properties of memristor- state retention or non-volatility. A read/write circuit is proposed which works based on this basic property. So, use of either linear or non-linear memristor model does not affect the performance of the read/write circuit. However, we have used a memristor emulator based on linear model; real memristors show nonlinear behavior because their fabrication technology has not matured sufficiently [20]. Also we have not used commercially available memristors (such as from KNOWM) because the commercial aspect of memristor is yet to be matured. The memristor state in this work is assumed to be the voltage across capacitor of the memristor emulator circuit; in fact, actual memristor state is obtained by multiplying instantaneous capacitor voltage by a fixed resistor and adding another fixed resistor as shown in Figure 2 [13].

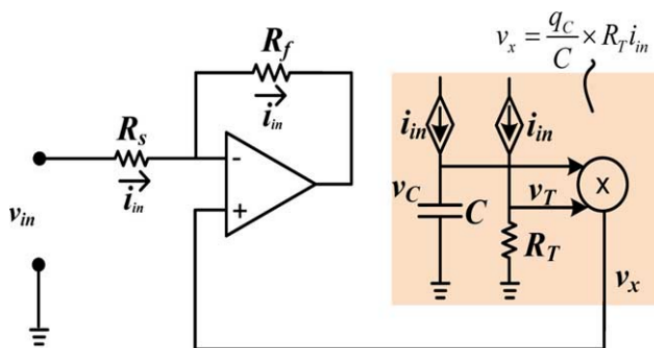


Figure 2. Design Philosophy of a Memristor Emulator [13].

## 1.1 Memristor State and Initial Condition

The voltage across capacitor at any instant of time is always proportional to the integral of the current through the capacitor.

$$v_c = \frac{1}{C} \int_0^t i(t) dt + i(0) \quad (1)$$

where  $i(0)$  is the initial current in the capacitor. Since integral of current is proportional to the charge, (1) can be written as

$$v_c = \frac{q_c}{C} + q(0) \quad (2)$$

$q_c$  is the charge at the capacitor at any instant of time and  $q(0)$  is the initial charge stored at the capacitor. Since memristor state is this capacitor voltage in our model, state in practical memristor can be achieved/matched with this kind theoretical state by changing the initial charge across the capacitor. For this, the capacitor can be biased at a fixed charge level by using a constant current source. MOS Field Effect transistors can be employed to design a constant current source.

## 1.2 Organization of the Paper

Rest of the paper is organized as follows: section II gives brief introduction of memristor linear model followed by the discussion of Kim's emulator. Section III discusses the proposed read write circuit and its operation. Simulation results of our memristor emulator based read write circuit is presented in section IV. Section V compares the efficiency of the proposed circuit with the earlier design. Finally, a short conclusion is given in section VI.

## 2 Principle of Memristor and Memristor Emulator Circuit

From a circuit perspective, memristor is often modeled as a two terminal device, with two electrodes and a sandwiched conductive channel which acts as a switching layer [3, 21]. In general the memristive systems are defined as [22]

$$\frac{dx}{dt} = f(x, u, t) \quad (3)$$

$$y = g(x, u, t)u \quad (4)$$

where  $u$  and  $y$  denote the input and output of the system and  $x$  denotes the state of the system. From (3), it can be seen that, in a memristive system the state evolves with time  $t$ . The equations can be modified by choosing appropriate variables to define memristor for electronic circuit as

$$\frac{dw}{dt} = f(w, v_M, t) \quad (5)$$

$$i_M = M(w, v_M, t)v_M \quad (6)$$

where  $v_M$  and  $i_M$  denote the current and voltage of the memristor and  $w$  denotes the internal state variable.  $M$  denotes the memconductance (memristance). As shown in (5) – the voltage input directly affects the state variable  $w$  – which is typical in first order memristive system [5].

Memristor linear model shows how memristance arises naturally in nanoscale system due to coupling of electronic and ionic transport under an external bias. Equivalent circuit for this model is shown in Figure 3. Two state dependent resistors are in series, and they represent ON and OFF channel resistance respectively.

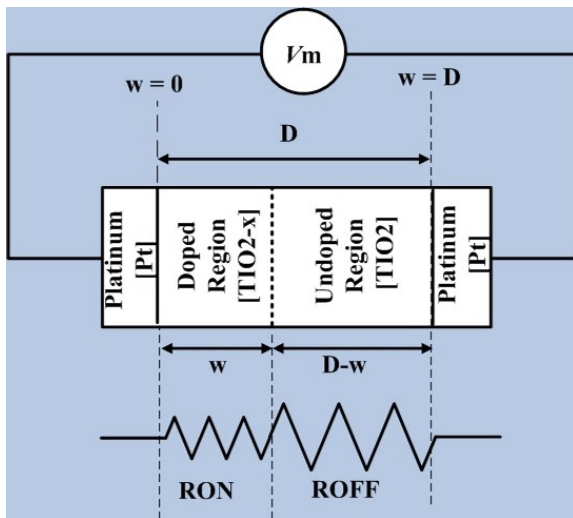


Figure 3. Linear Memristor Model.

The device dynamics and the  $i$ - $v$  characteristics are described by (7) and (8) respectively.

$$\frac{dw}{dt} = \mu_v \frac{R_{ON}}{D} i_M \quad (7)$$

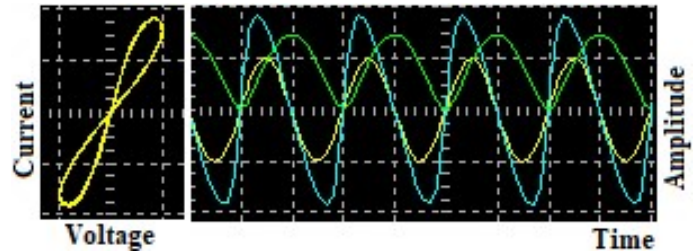
$$v_M = \left( R_{ON} \frac{w}{D} + R_{OFF} \left( 1 - \frac{w}{D} \right) \right) i_M \quad (8)$$

where  $\mu_v$  is average ion mobility,  $R_{ON}$  is the resistance of doped region,  $R_{OFF}$  is the resistance of undoped region, and  $w \in (0, D)$ . This model considers ohmic electronic conduction and linear ionic drift, and assumes modulation of  $w$  is due to drift of charged dopants [3].

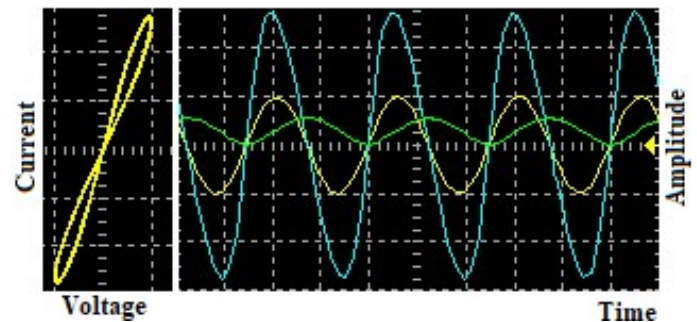
The incremental configuration of memristor emulator [13] is used in this work. One of the distinguished features of Kim's emulator is that the memristor can be programmed by giving pulse input and the programming information can be stored in the capacitor for longer period of time. This feature of memristor is important to use memristor as a computational memory element [23]. To confirm the basic memristor properties, 1 volt sinusoidal waveform is given at frequencies of 100 Hz and 400 Hz respectively. Current probe with voltage to current ratio of 1 V/mA is used for plotting the current trace in oscilloscope. Oscilloscope traces are shown in Figure 4. Increased height with increment in frequency in the pinched loop confirms incremental configuration of the memristor. In the time domain, green trace is voltage variation across the capacitor, and this voltage is considered as memristor state in our work.

The response of memristor with programming pulse input is shown in Figure 5. In all the four cases (Fig. 5a, Fig. 5b, Fig. 5c, Fig. 5d), the increment step size is smaller as more pulses are applied. This is because, in a memristor present state is the cumulative effect of past applied pulses. This observation leads memristor to be useful as a computational memory element particularly for neuromorphic computing. Non volatility of the memristor state during inter pulse period can also be seen.

The results in Figure 4 and Figure 5 are consistent with the results obtained in [13].



(a) Pinched hysteresis loop at 100 Hz and corresponding time domain waveform.

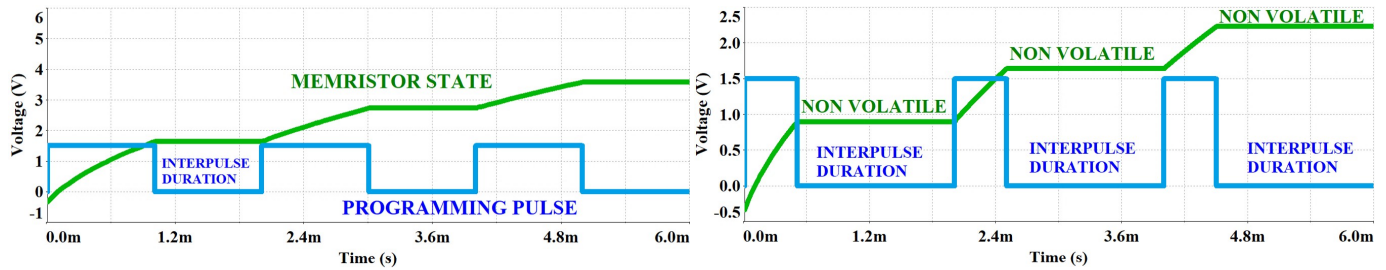


(b) Pinched hysteresis loop at 400 Hz and corresponding time domain waveform.

Figure 4. Response of Memristor Emulator in XY and YT Mode of an Oscilloscope. In the time domain, yellow trace represents input voltage, green trace represents voltage across capacitor, and blue trace represents waveform generated by current through memristor. Time axis is at 5 ms/div. In YT mode, yellow trace is at 1 V/div, blue trace is at 50 mV/div, and green trace is at 2 V/div.

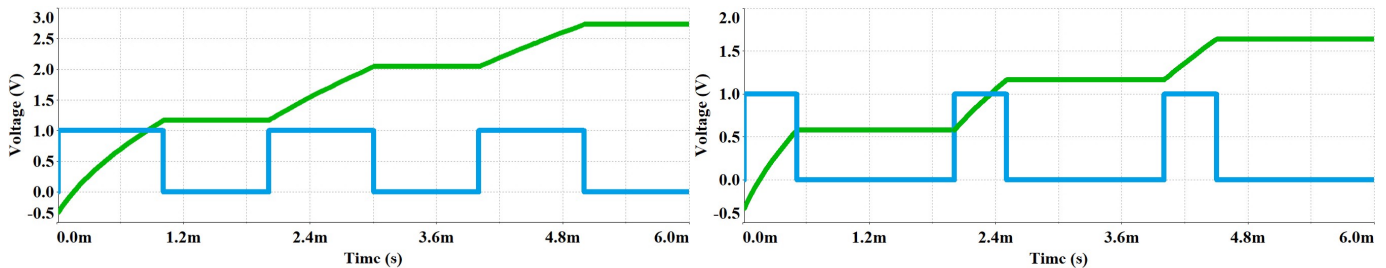
### 3 Proposed Read Write Circuit

Based on memristor response to pulse input, a read write circuit is proposed in this paper. The block diagram of the read write circuit is shown in Figure 6. The comparator is used for detecting the state of the memristor (high or low) depending on the nature of programming pulse. The maximum and minimum voltages that can be written in the memristor are 5 volts and 0 volt respectively. The read circuit should read high/low, after the read pulse is given. When the memristor state voltage is above 2.5 volts, the read circuit should read high (5 volts). Similarly, when it is below 2.5 volts, the read circuit should read low (0 volt). The read circuit should perform two tasks: first, it should detect read pulse and activate read circuit; second, it should compare the output voltage of memristor with



(a) Change in memristor state with 1.5 volts amplitude programming pulse. The programming pulse has equal ON and OFF time duration.

(b) Change in memristor state with 1.5 volts amplitude programming pulse. The programming pulse has ON time less than OFF time.



(c) Change in memristor state with 1 volt amplitude programming pulse. The programming pulse has equal ON and OFF time duration.

(d) Change in memristor state with 1 volt amplitude programming pulse. The programming pulse has ON time less than OFF time.

**Figure 5.** Effect of Variation of Height and Width of the Programming Pulse on the State of the Memristor.

2.5 volts to detect correct memristor state (high or low). If there is no read pulse, the read circuit should not come into action, and the read circuit should retain its original state. Any bipolar pulse with zero average value could be chosen to read from memristor without perturbing its internal state.

Flow chart in Figure 7 depicts the general operation of read write circuit. The detailed circuit diagram of proposed memristor emulator based read write circuit is shown in Figure 8. The circuit consists of a PMOS transistor, a resistive attenuator, and two high gain operational amplifiers. The circuit is developed based on Figure 6 and Figure 7. Q1 and first comparator serve the purpose of detecting bipolar pulse and activating read circuit. Resistive attenuator is formed by two 1 kilo ohms resistors. The final comparator compares memristor current state with 2.5 volts and gives single bit output (high or low). One of the unique features of this circuit is that it does not need external read write enable switch to toggle between read write operations, instead this is achieved by unipolar write pulse and

bipolar read pulse.

### 3.1 Analysis of the Proposed Read Write Circuit

The PMOS transistor in the circuit of Figure 8, Q1, has same specifications as the specifications of the transistors used for developing memristor emulator. The threshold voltage ( $V_t$ ) is -0.5 volt and device constant (K) is 1 mA/V<sup>2</sup>. The gate voltage ( $V_G$ ) becomes positive with respect to ground during entire write cycle due to positive unipolar nature of write pulses. Since the read pulse is bipolar, the read circuit activates only during negative interval of the read cycle.

When the input pulse is positive, for example +1 V, the transistor remains in saturation region. The source potential ( $V_S$ ) is computed as [24],

$$(5 - V_S) = \frac{1}{2}K[V_{SG} - |v_t|]^2$$

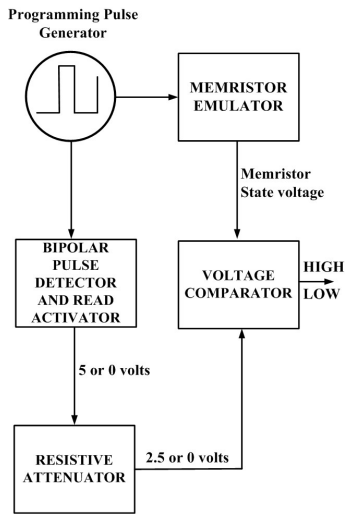


Figure 6. Block Diagram of the Proposed Read Write Circuit.

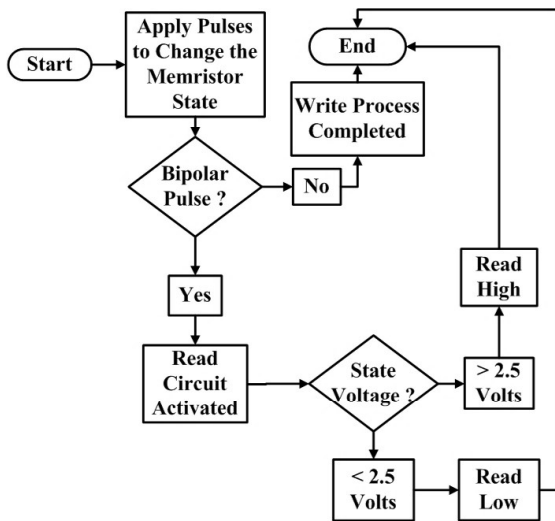


Figure 7. General Idea Depicting Operation of the Read Write Circuit.

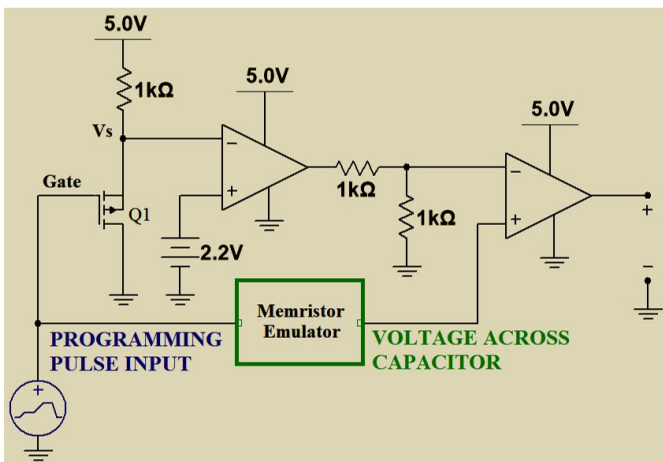


Figure 8. Proposed Read Write Circuit.

$$(10 - 2 \times V_S) = [V_S - 1 - 0.5]^2$$

$$V_S = 3.32V$$

When the input pulse is negative, for example, -1 V volt, the transistor enters into the triode region. Neglecting channel length modulation effect, the source voltage is computed as,

$$(5 - V_S) = K \left[ (V_{SG} - |v_t|) \times V_{SD} - \frac{V_{SD}^2}{2} \right]$$

$$(5 - V_S) = [(V_S + 1 - 0.5) \times V_S - 0.5 \times V_S^2]$$

$$V_S = 2V$$

If  $V_S$  is above 2 volts, memristor is in write mode and vice versa. Leaving 0.2 volts as safety margin, the source voltage is compared with 2.2 volts to detect read pulse and read duration.

$$\text{Memristor Mode} = \begin{cases} \text{Write,} & \text{if } V_S > 2.2 \text{ V} \\ \text{Read,} & \text{if } V_S < 2.2 \text{ V} \end{cases} \quad (9)$$

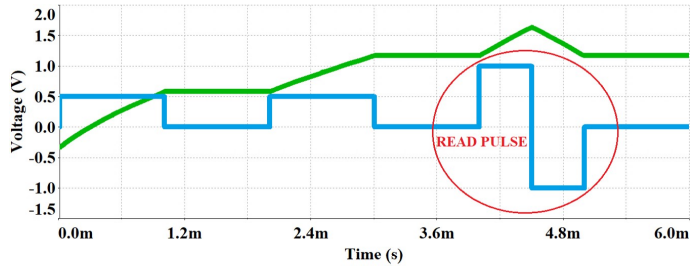
The output of first comparator goes high only when the read pulse is detected; this leaves negative terminal of second comparator at 2.5 volts. By comparing memristor state with this 2.5 volts, final output is taken as the state of memristor from the second comparator.

## 4 Experiments and Simulations

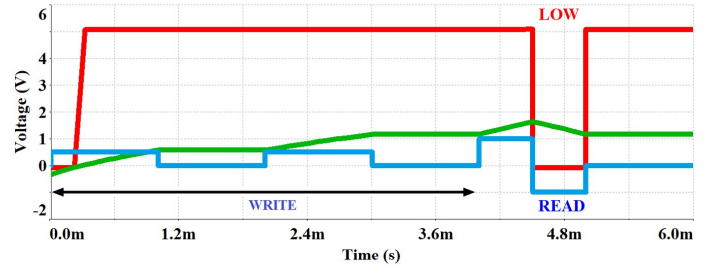
A read write circuit is designed using memristor emulator based on the linear memristor model. Internal state of the memristor should not be disturbed by the read cycle; it shall return to its original state after the completion of read cycle. Simulation has been performed on the read write circuit by applying zero average and non-zero average read pulse. From the simulation results, it is seen that in zero average pulse the memristor state returns to its original state, which does not happen with non-zero average pulse. In Fig. 9a, memristor returns to its original state of 1.2 volts after the application of zero average pulse; whereas, memristor fails to return to its original state with non-zero average pulse as shown in Fig. 9b. Therefore, zero average bipolar pulse is chosen as a read pulse.

If the state of the memristor is below 2.5 volts, the output of the read circuit is zero for the read duration. Similarly, if it is above 2.5 volts, the output of the read circuit is 5 volts. The complete response of the memristor emulator based read write circuit is shown in Figure 10. Originally, the output of the read circuit is 5 volts. When the low state is detected, it jumps to the low state (0 volt) as indicated in the Fig. 10a. If high state is detected during the read cycle, output of the read circuit does not change its original state as indicated in the Fig. 10b. Green trace represents memristor state voltage. Blue trace represents programming and read pulse. Red trace represents logic generated by the read write circuit.

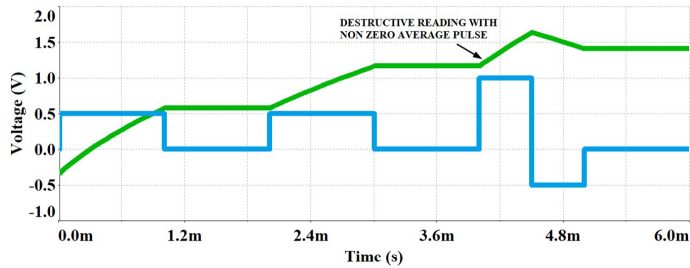
During read cycle, the state of memristor changes; however, at the end of read cycle the memristor should return to its original state. The read duration is deliberately chosen as negative state of the read pulse. Due to read cycle distortion, the memristor may enter into incorrect state. Therefore, in order to



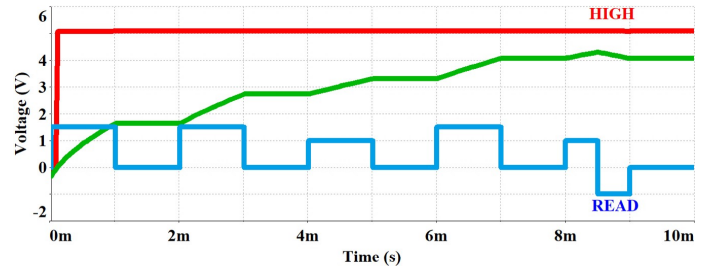
(a) Returning of memristor to its original state with zero average bipolar read pulse.



(a) Reading low by the read circuit. The state of the memristor is below 2.5 volts.



(b) Memristor fails to return to its original state with non zero average bipolar read pulse.



(b) Reading high by the read circuit. The state of the memristor is above 2.5 volts.

**Figure 9.** Effect of Zero Average and Non-zero Average Pulse on the State of the Memristor.

**Figure 10.** Read Circuit Reading Low and High Memristor State During Negative Cycle of the Bipolar Read Pulse.

preserve the data integrity, state of the memristor is read at the negative half of the read pulse. As shown in Figure 11, due to the read cycle distortion, the state jumps above 2.5 volts (falls on the false region), but the state is correctly read as low during negative state of bipolar read pulse preserving data integrity. Therefore, the designed read circuit is not only simple and non volatile but also resilient to read cycle distortion.

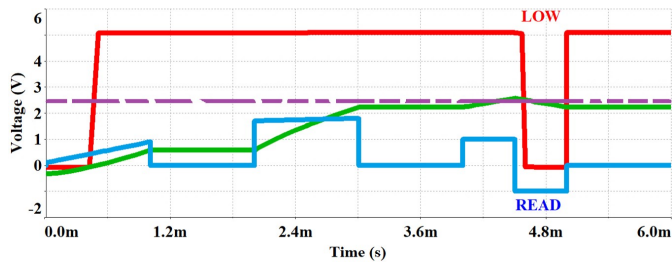
is very large compared to MOSFET, the efficiency of MOSFET based switch is higher compared to diode based switch. In the context of Switch Mode Power Supplies (SMPS) in [25], the author has shown the percentage power loss in diode as 15.5% and in MOSEET as 8.3%. In Table 1, we have shown the efficiency comparison.

## 5 Efficiency Comparison

The overall efficiency of the read/write circuit depends on the efficiency of the switching device. We have used N type E-MOSFET as the switching element in the proposed read/write circuit. The switching efficiency greatly enhances if the MOSFET is used in full cut-off and deep triode region because power dissipation in these two regions is extremely low. Read/write circuit in [12] uses diode as a major switching element. Since the ON channel resistance ( $r_{DS(ON)}$ ) of a diode

**Table 1.** Efficiency Comparison of Diode and MOSFET Based Read/Write Memory Cell

	Switching Device	$r_{DS(ON)}$	Power Loss	Efficiency
Ref [12]	Diode	High [25]	High	Low
This Work	NE-MOSFET	Low [25]	Low	High



**Figure 11.** Reading at the Negative State of Read Pulse to Prevent False Reading Due to Read Cycle Distortion.

## 6 Conclusions

The application of memristor as a memory element has been explored through a memristor emulator based memory cell. In this paper, we have designed and developed a read write circuit based on memristor emulator, which can read a single bit. Similarly, the circuit can be taken to any states between 0 to 5 volts representing different memory states. With unipolar write pulse and bipolar read pulse, the circuit can be switched between read and write operations without using an external read/write enable switch.

The read write operations of the proposed circuit are analyzed to ensure the non volatility of the memristor states. Furthermore, the possible read distortion is analyzed and the read access time duration in read pattern is proposed to preserve data integrity during the read cycle.

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