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Dynamic WIP Management with the BullWIP Situation for Semiconductor Fabrication Foundry

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Abstract Complementary Metal Oxide Semiconductor (CMOS) is a complex and very delicate process in semiconductor. In typical 30,000 wafer capacity of single foundry business model, the CMOS product loads are mixed from various technologies to serve wider market segments. Total devices can be ranged from 100 to 200. This approach creates variables for process time, equipment usage, number of processing steps which leads to inconsistent WIP profiling at respective time period. Approach to maximize the output is used by changing the methodology of WIP movement through a good WIP Profile chart management. A dynamic WIP management approached can improve the FAB out ~ 5%. It will also help the factory to make a right decision to manage the WIP balancing especially when we face BullWIP situation. The Production Control will get a good benefit from this study. A linear plan is no longer work in managing BullWIP situation and an approach on how to improve the line balancing is required.

Keywords Day Per Mask Layer (DPML), Work in Progress (WIP), WIP Profile, CMOS, Foundry

1. Introduction

Semiconductor manufacturing is the most complex manufacturing process in the world. Semiconductor manufacturing is a multistage process which transfers silicon in the form of thin, polished wafer into integrated circuits. The entire process basically includes four main steps: Raw wafer manufacturing, wafer fabrication, probe and die, package and test. Wafer fabrication is most time-consuming and complicated one, consisting primarily of at least six major types of phases or module: Diffusion, Lithography, CVD, Thin Film, Etching and Ion Implantation. The wafers passing through these six major modules numerous times. The fabrication of a wafers is typically from 45 to 60 days. The entire fabrication process involves hundreds of operation steps performed on a variety of machines. Wafers are grouped in lots and transferred in a standard cassette. A wafer must visit some machine groups more than once. The process is typically consists of re-entrants process through many resources.

For instance, a wafer may need to visit photolitoghraphy module 20 to 38 times for all layers of circuitry to be fabricated. This complexity of the wafer fabrication process caused wafer release and dispatching decisions are extremely difficult to be achieved. It result to poor cycle time if the dispatch is not optimized[1].

The maximization of critical resource utilization as well as throughput rate and the minimization of cycle time are the primary goals of the release and dispatching policy in wafer fabrication because of its capital-intensive nature and the need to attain a competitive advantage [2].

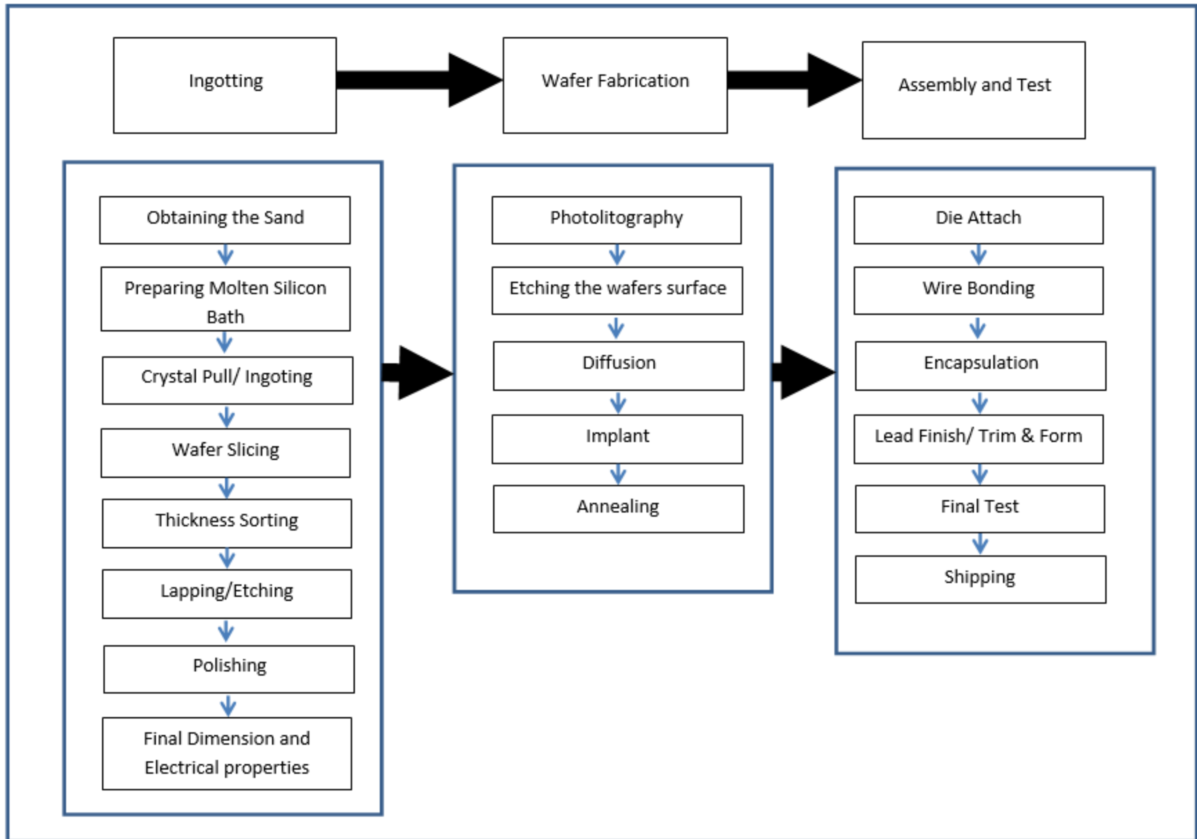


Figure 1. Semiconductor Flow from Ingotting, Wafer Fabrication and Assembly Test

Wafers generally move through in lots in a wafer fabrication factory. The operational batch sizes range from a single wafer to several lots. Processing times depend mainly on the operation types. For a single wafer processing tools like photolitoghraphy, the processing time depends on the number of wafers in a lot. For batch processing operations like Diffusion, no matter how many lots are loaded at a time (the number of lots batched must be smaller than the maximal batch size which is usually 6 lots or 150 wafers), the processing time generally does not vary with the number of lots batched.

There are many characteristics of wafer fab like in Fig. 2, such as re-entrance processing flow, batch tools, sequence dependents set up, unpredictable equipment failure and so on, which differentiate wafer fab from other traditional flow shop or job shop. Normally, release strategy and dispatching strategy are two major ways which are applied to control the wafer fab with the puzrpose of decreasing average cycle time and cycle time variance, achieving on time delivery of the products. Many methods were used on applying the dispatching strategy to wafer fab.

As the process are too complex, automation methods used to improve the productivity and managing the Work In Progress (WIP) materials. There is strong correlation between cycle time and the factory utilization. As the utilization increase, the cycle time may deteriorate. With the WIP increase, the queue time to process will also increase.[3]

Due to the delicate semiconductor process, the high queue time to process will increase respective process especially at higher re-entrance level[4]. Cycle time in wafer fabrication is measured by day per mask layer (dpml). It is a method to measure the re-entrances at lithography process.

Day Per Mask Layers is an indices in wafer fabrication industry to monitor the cycle time (CT) or Turn Around Time (TAT). It is measuring by the average of the mask layers being processed during the fabrication step. Mask is the circuitry design to print on the wafers during the fabrication process. It has multi layers during the lithography or stepper process.

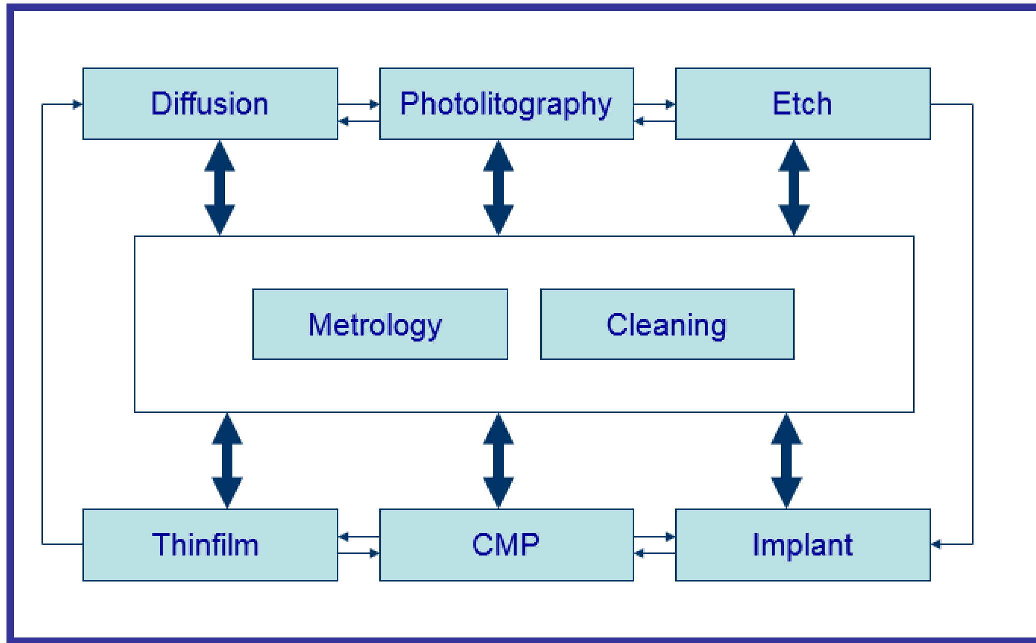


Figure 2. Typical Wafer Fabrication Process

Bull WIP Situation

Bull WIP situation happen when there is high WIP at a particular step or process. The BullWIP can happen due to:

1) High WIP at BN areas.
2) Poor process or tools performance
3) Poor BN Management.
4) Over capacity. Load above capacity.

Although the bottleneck is the most critical work center which determines the performance of the whole fab, feeding empty non-bottleneck work centers can also smooth the material flow, avoid capacity losses of machines, and improve product cycle times[1]. Therefore, a minimum workload 1.5 hours is also defined for the non-bottleneck work centers. If the workload of non-bottlenecks drop to this minimum workload level, lots are scheduled to feed it to avoid starvation.

Production Control (PC) will assign the layers output for each process. Production Control main function is to ensure the On Time Delivery (OTD) for each devices and volumes for each Customers are met. Production Control has the privilege to upgrade and downgrade the lots to ensure the OTD are protected. At the same time PC will also has the function to control the WIP movement. PC will apply the Line Balancing concept to maximize the moves and utilization by applying Starvation Avoidance concept to ensure there is no resources are idle. PC function as FAB planners are very critical and important to make sure the resources are busy and moving the right WIP. PC will be responsible for the resources' daily planning move and output.

In typical Integrated Module (IM) activity, PC will assign moves or output for each IM based on the resource capacity and the capability to the IM to produce the moves or the output. Due to the re-entrants process, PC will assign a balancing target moves or output for each layer. The plan is done through manual calculation and it will be uploaded to the system to track the moves and the output. A report to monitor the output hourly will be automated through email and the reporting system to ensure the right layers and moves or output achieved.

The Line Balancing concept is important and by developing the WIP Profile report, it will help the PC and Manufacturing Manager to manage the WIP movement. Since the processes are re-entrants, any spike WIP in the WIP Profile show the real time issue face by the line. It can be due to tools downtime, or WIP congested due to capacity constraint. In the study, M. A. Chik et al. [5] states that applying Bottleneck Management (BN) concept or Theory of Constraint (TOC) is deem needed to ensure the BN resources which determine the FAB capacity are fully loaded with WIP. At the same time it is also important to avoid high WIP waiting at the BN resources. The PC function is important to avoid the WIP pile up and queue in front of the BN resources by moving the WIP to resources that starving or idle.

2. Dispatching Management and Developing Line Balancing Mechanism

In developing a line balancing monitoring, we have to review the overall factory WIP. A profile of WIP distribution to indicate the inventory level of each steps or

stages will help the Production Control (PC) and Factory Manager (FM) to manage the production floor effectively. The facts that a resources have to run multiple layers or the process re-entrant to the tools need a very systematic approach both in the dispatching system as well as the output plan.

PC will use a layer plan system to determine number of moves required for each layers and will map with the resources capability to meet the plan output or moves. The layers plan system will use the wafer per hour (WPH), equipment availability and utilization from the Industrial Engineering data base (IEDB) to match the moves requirement. In the case of BN area, K. Ibrahim [6] state that maximizing the moves will help to optimize the factory output. A close monitoring moves plan requirement is set by the PC.

At the same time the Manufacturing System Engineers will work on the right methodology to determine the best dispatching method to ensure a proper layer plans for each steps. The combination of the layer plans given by the PC, BN management and Due Date for each lots and device will automate the lots sequencing for the operators. It will improve the factory utilization and increase the factory output.

The dispatching system will also improve to optimize a good batching system and it will benefit a good cascading to run the process and equipment [7].

In order to monitor the WIP balancing, PC will assign layers plan move to each areas and process.

The FAB WIP is divided to 7 different segmentations. It will make the plan more systematic.

1) Pre Poly 1 - From Wafer dispatch to STI Anneal
2) Pre Poly 2 - From HNwell Mask to PWell Anneal RTP
3) Poly - From MVGate Pre Clean to Poly Etch
4) Post Poly 1 - From Poly ReOx Pre Clean to Spacer Nitride Etch Resist Strip
5) Post Poly 2 - From NSD Mask to ILD CMP
6) Backend - From Contact Mask to Top IMD CMP.
7) Final - From Top Via Mask to Finish Good

The FAB WIP is divided to 7 sub areas for better management. Each areas is given the specific target based on:

a) Area WIP level
b) The Area average mask level
c) The Area Moves Plan
d) The Area Turn Ratio
e) The Area CT plan

2.1. PrePoly One (PreP1)

PreP1 started from wafer loading to the Nitride Strip process. With average 4 masks level a longer CT is expected at Prep1 due to reentrants for Diffusion Furnace process. Diffusion is a batch process and the process duration from 8 to 12 hours. PreP1 has 6 Diffusion steps.

2.2. PrePoly Two (PreP2)

PreP2 started from HNWell Mask to Pwell Implant Resist Strip process. PreP2 typically has 10 mask layers mainly the reentrants for Implantation process. The wafers typically moves between Photolithography, Implant and Cleaning. Wafers are moving fasters at this area even though Photolitography is the bottleneck for the FAB.

2.3. Poly

Poly module started from Gate Oxidation 1 or MV Gate Oxidation process to Poly Etch process. Poly typically has 3 mask layers. Poly also consist 4 Diffusion Furnaces step. Due to the longer furnaces process, the process cycle time at this area is designed to be longer.

2.4. Post Poly 1 (PstP1)

PstP1 started from the NLDD Mask layer to Spacer Nit Etch. PstP1 also has 8 Implants step with 5 mask layers. The theoretical cycle time is shorter and will generate fast WIP turn.

2.5. Post Poly 2 (PstP2*)*

PstP2 started from NSD mask layer to ILD CMP process. PstP2 has 3 mask layers. Consist of 3 Implant mask layers and multiple thin film deposition layers. It is also consist 1 Chemical Mechanical Polishing (CMP) layer.

2.6. Backend (Backend)

Backend started from Contact Mask to Top IMD CMP. Backend has 9 mask layers and multiple re-entrant processes between Photolitography, Etch, Thin Film and CMP. Backend is single wafer processing type of tools. Theoretical Cycle time is faster at backend.

2.7. Final

Final started from Top Via Mask to Shipping. Final has 3 mask layers. The completed processed wafers required to run through electrical test process. Wafer Acceptance Test (WAT) is a routine run test for every wafer where the wafer will be electrically tested. A test structure is designed at the scribe line to electrically confirm our process. Good wafers will be thoroughly inspected by the Outgoing Quality Assurance (OQA). If there are no abnormalities found, the good wafers will be packed and ready for shipment to the customer’s location.

But the zonal WIP management is an approach to enhance the current method. The fact that wafers run through re-entrants at most of the process, a new systematic way to manage the WIP has been discussed. By having the zonal WIP profile management, we can quick to identify whether the real bottle neck (BN) is

really occupied with high WIP.

In a real wafer fab, the material flow is generally nonlinear due to different events such as unpredictable tool failure, batch processing, setup change, process dedication and so on [8]. Thus WIP fluctuation occurs frequently, especially lots pile up in front of tool group during downtime period. In that case lots spend hours, even days in the queue if there is no appropriate scheduling. This accumulated WIP in front of a certain tool group causes WIP imbalance for the whole line, which has great impact on cycle time as well as on time delivery [9].

Sometimes due to equipment availability issue, and also the process limitation due to tight margin, a temporary BN exist in the WIP profile. Spike WIP can be seen clearly and an orchestrated effort from the Engineering team is required to improve the constraint. A group of engineers and the Manufacturing team will look at the alternative way to improve the situation [10]. A small changes in the dispatching system is required by the Manufacturing System team to avoid WIP piling up at the temporary BN areas [4]. The upstream WIP will be channeled to the less WIP areas through the Starvation Avoidance (SA) method.

P. Balakrishna et al. [11] in their study, found that higher queue time for the wafers to be processed at the temporary BN will impact the overall FAB cycle time. It will also cause capacity lost if the FAB BN area is idle. A dynamic WIP movement management coming from the dispatching system will be complimented if we know the WIP situation. Having the New WIP Profile management will help the production supervisor to make a quick decision on how to handle the incoming WIP.

3. Implementation and Discussion

3.1. Developing a Dispatching System

J. K. Robinson and F. Chance [12] proposed to manage wafer fab cycle time using MES data. Fig 3 shows how the MES link to a few servers to create a dispatching system that will have to enable the operators to plan their lots sequencing and loading.

With the help from CIM and Manufacturing System Engineers, a good dispatch system was establish [13]. The global and local rules are implemented to ensure the On Time Delivery and Optimizing the factory revenues with a good BN management is in place [5].

In Fig 4, a WIP control strategy will help to ensure the factory BN will always busy and no capacity loss due to idle [14]. A good dispatch system with starvation avoidance rules will ensure the factory produce as per the capacity [15].

Capacity of the factory depend on the BN performance. It is mandatory for factory manager to ensure the BN machines are fully utilized.

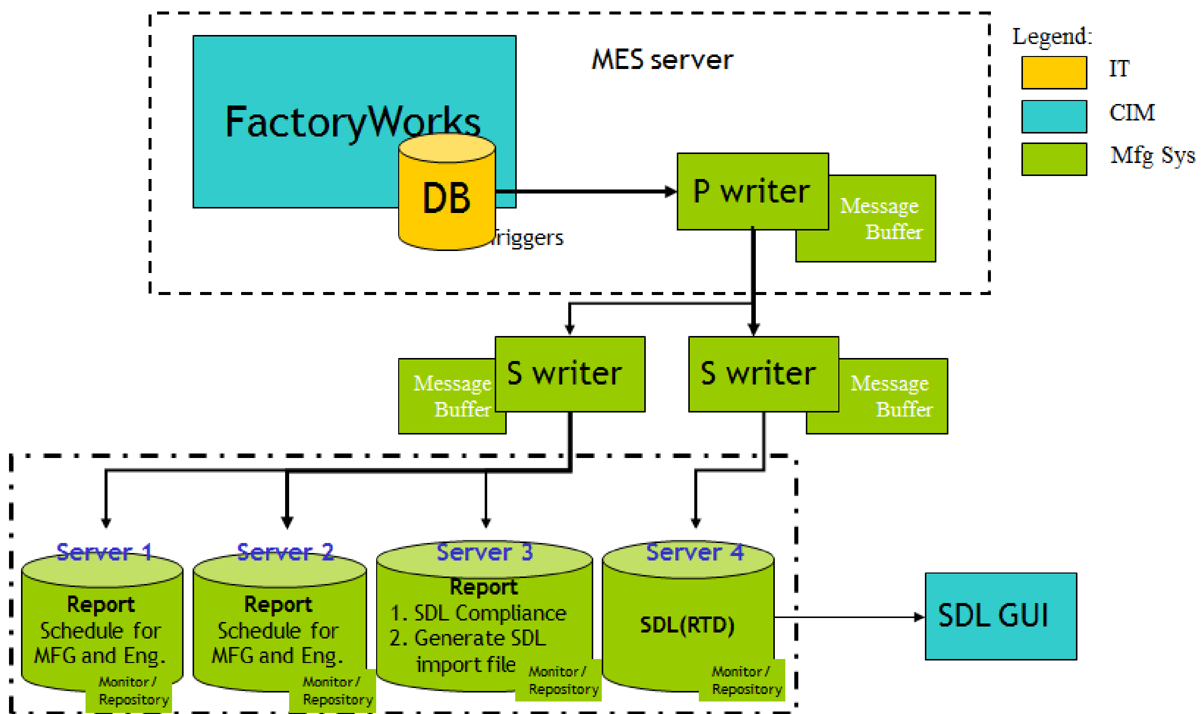


Figure 3. Diagram of Real Time Dispatcher Architecture

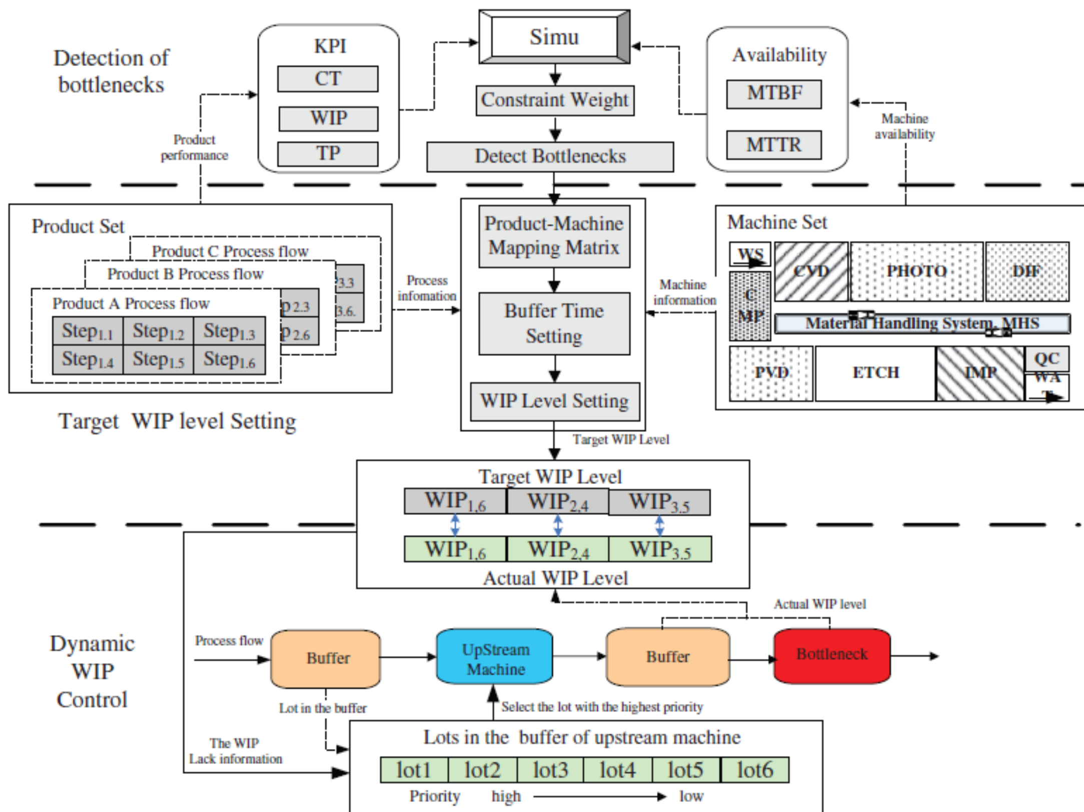


Figure 4. WIP Control Strategy

Fig.4 is an example of the method used by H.Hu et al. [16], on how he strategized his dispatching policy. The control of the WIP method at the BN area. When BN area have sufficient WIP, the dispatch will moves the priority to next resources.

A global rule is set in the factory dispatching rules. It will govern the factory wide lot movements by:

1) Lot Priority
2) Shipment due date.
3) Starvation Avoidance for BN area.
4) Critical Ratio

Above are parts of global rule used to determine the overall factory dispatching system. But for each individual areas and resources, there is local rules allowed to maximize the output of the equipment and the factory.

Local rules consist of:

- Running in a batch
- Running same recipe
- Based on species when it is related to the life of the part, chemical or gas.
- Based on Preventive Maintenance schedule.
- Based on the incoming WIP
- Based on internal customers or process needs.

A dispatch system that build in the factory is required to ensure standardization since information cascade to the production floor will not be same page to deliver important instruction from top to operators [17]. Do not have visibility of incoming WIP or next area WIP. Do not sure which equipment has recipe release Do not sure which tool is the process preferred to run (yield, cost) Do not have visibility of issue placed at next step .Need longer time to track others wafer (PRD and test wafer) that needed to be batch together for optimum output and move. Poor visibility on the high age lot, important rework lot, ILP lot. Not executing required lot by Production Control request. Do not have visibility when is the right time to do PM.

3.2. Developing a WIP Profile Management

J. Lee et al. [18] in the study state that Manufacturing Execution System (MES) mainly used to manage WIP and equipment automation in the FAB. Huge amount of data are recorded automatically in multiple databases during fabrication process where the data become the input to monitor lot movements in the semiconductor fabrication plant, or shortly FAB. MES database composed of a collection of sub systems, each with a specific task contributes to huge database because every single transaction needs to be recorded [18].

In Fig.5, the WIP Profile has been designed using the concept of small data warehouse by understanding and analyzing the business needs in this FAB. Based on the current framework and the application layout, the report generator architecture has been constructed using the concept of top down view as shown in Fig. 5 below. This approach will select only the relevant information needed for faster data retrieval and accuracy.

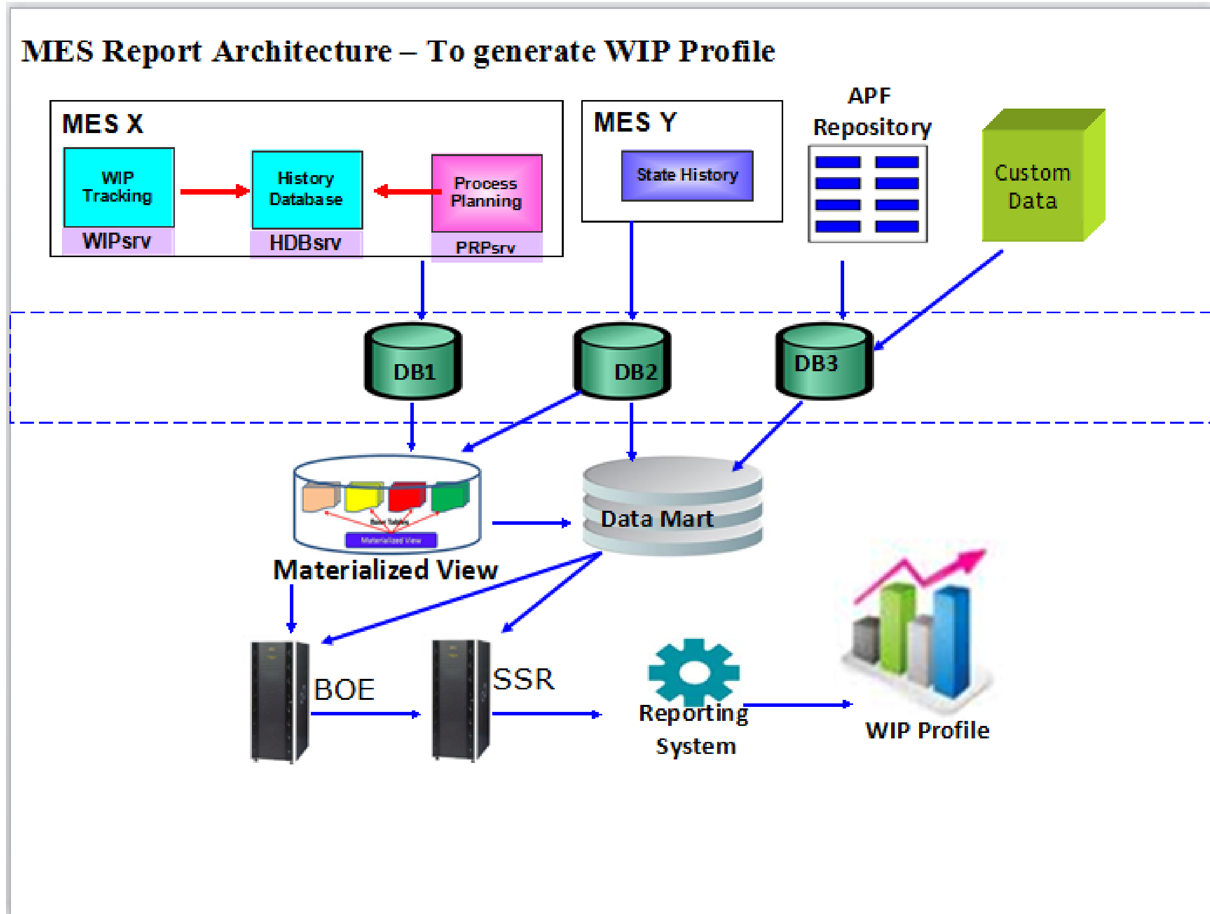
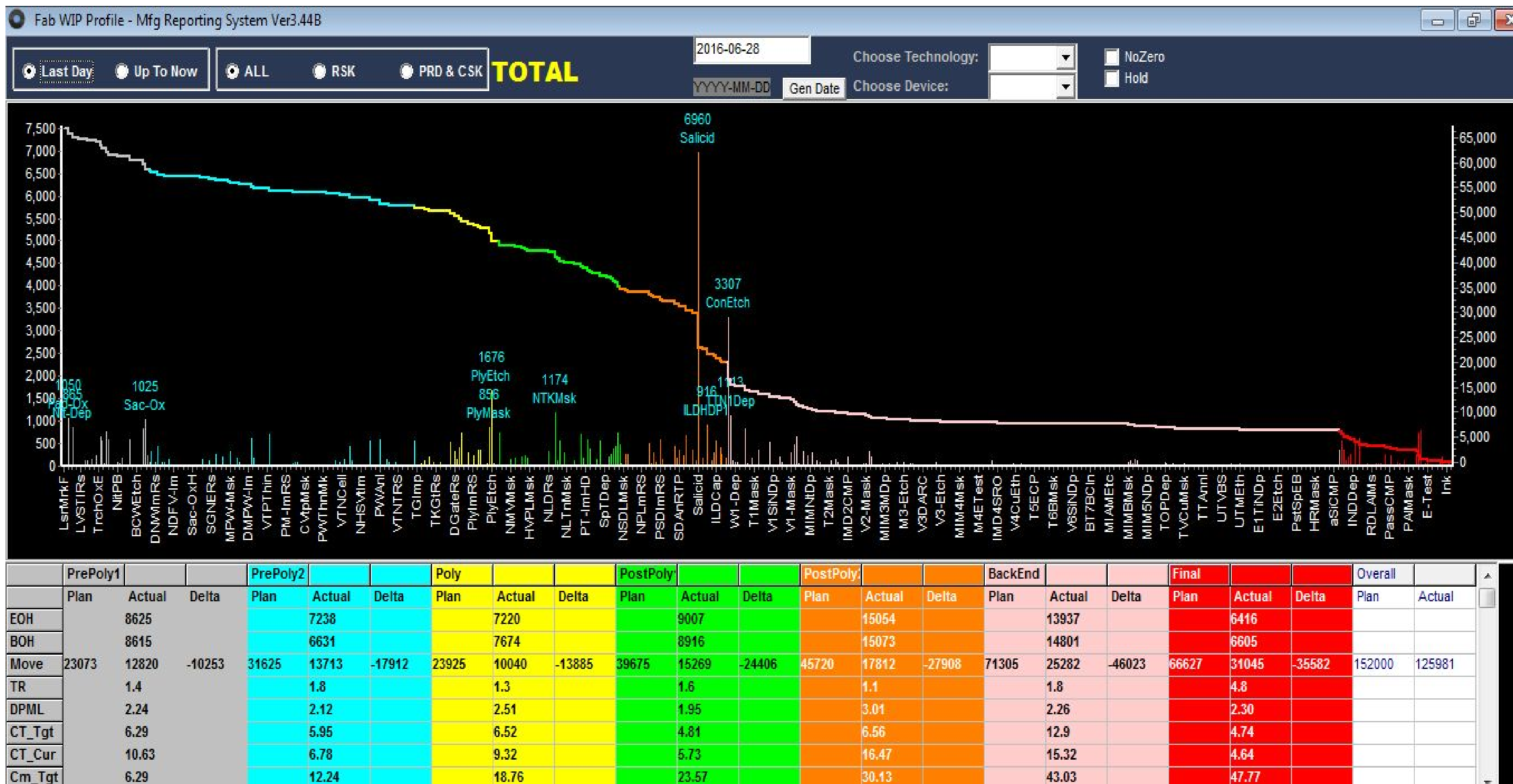


Figure 5. MES Architecture in Developing the WIP Profile Report

The data retrieves mainly from MES application to get the WIP, movement and process flow information. This data will be consolidating with other external application that is APF repository data. In addition, external custom data from the user also will be used for this process. Data from multiple databases will be on cleansing, de-duplication and transformation to more reliable and meaningful data. In this design, we are using a query to summarize the data and it will be store into a data mart. Materialized view concepts also have been used for efficient data retrieval. Materialized views have been found to be very effective in speeding up query as well as update processing [19]. A few server have been schedule to run the automated jobs to generate the summarize data. Users are able to view this information through web page, Reporting System or even email.

The output of the system is the WIP profile with the zone and it will give us a better line balancing visibility and with the FAB divided to 7 different zone for better management.

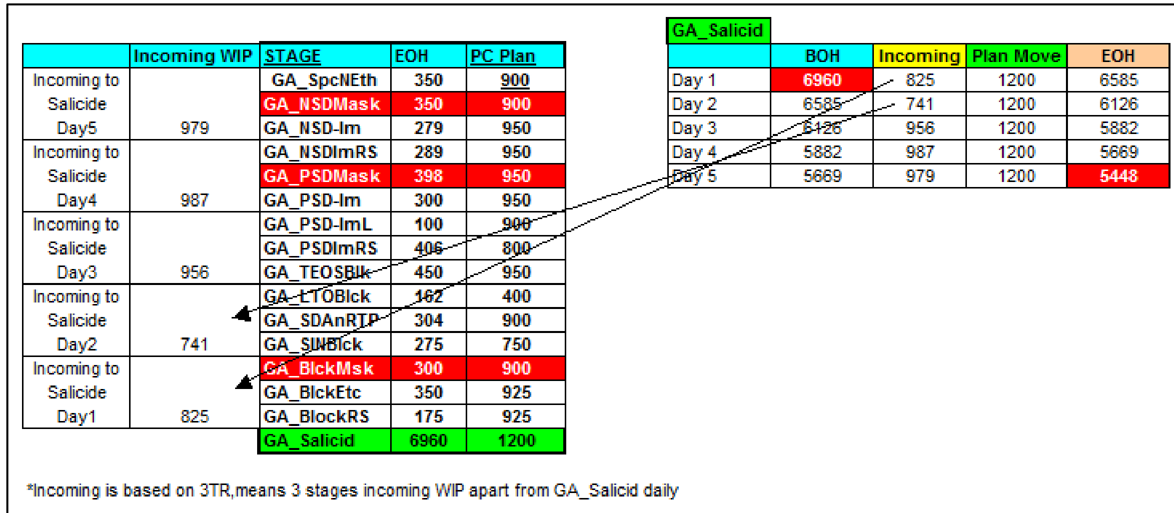
3.3. WIP Profile to Manage BullWIP



	PrePoly1			PrePoly2			Poly			PostPoly			PostPoly			BackEnd			Final			Overall	
	Plan	Actual	Delta	Plan	Actual	Delta	Plan	Actual	Delta	Plan	Actual	Delta	Plan	Actual	Delta	Plan	Actual	Delta	Plan	Actual	Delta	Plan	Actual
EOH		8625			7238			7220			9007			15054			13937			6416			
BOH		8615			6631			7674			8916			15073			14801			6605			
Move	23073	12820	-10253	31625	13713	-17912	23925	10040	-13885	39675	15269	-24406	45720	17812	-27908	71305	25282	-46023	66627	31045	-35582	152000	125981
TR		1.4			1.8			1.3			1.6			1.1			1.8			4.8			
DPML		2.24			2.12			2.51			1.95			3.01			2.26			2.30			
CT_Tgt		6.29			5.95			6.52			4.81			6.56			12.9			4.74			
CT_Cur		10.63			6.78			9.32			5.73			16.47			15.32			4.64			
Cm_Tgt		6.29			12.24			18.76			23.57			30.13			43.03			47.77			

Figure 6. Bull WIP Profile

Based on the above WIP profile, BullWIP area is at Salicide stage. Daily capacity for Salicide is 1200, with sufficient WIP,PC will plan 1200 move. There are incoming WIP to this stage. The incoming WIP is based on 3TR,meaning in one day there are 3 stages cumulative WIP will come to Salicide. Attached is on how PC will plan the incoming and projected Salicide WIP after 5 day:



	Incoming WIP	STAGE	EOH	PC Plan
Incoming to Salicide Day5		GA_SpcNEth	350	900
		GA_NSDMask	350	900
	979	GA_NSD-Im	279	950
Incoming to Salicide Day4		GA_NSDImRS	289	950
		GA_PSDMask	398	950
	987	GA_PSD-Im	300	950
Incoming to Salicide Day3		GA_PSD-ImL	100	900
		GA_PSDImRS	406	800
	956	GA_TEOSBlk	450	950
Incoming to Salicide Day2		GA_LTOBlck	162	400
		GA_SDAnRTP	304	900
	741	GA_SINBlck	275	750
Incoming to Salicide Day1		GA_BlckMsk	300	900
		GA_BlckEtc	350	925
	825	GA_BlockRS	175	925
		GA_Salicid	6960	1200

GA_Salicid	BOH	Incoming	Plan Move	EOH
Day 1	6960	825	1200	6585
Day 2	6585	741	1200	6126
Day 3	6126	956	1200	5882
Day 4	5882	987	1200	5669
Day 5	5669	979	1200	5448

*Incoming is based on 3TR,means 3 stages incoming WIP apart from GA_Salicid daily

Figure 7. Bull WIP layer plan management

Salicide currently have 6960 WIP in front of the tool, there are 825 WIP expected will come to this stage in same day, called incoming WIP to Salicide Day1.Based on the projected incoming WIP, and daily move 1200 out from Salicide, after 5 days the WIP will drop from 6960 to 5448. Fig 7 shows how PC put the plan to ensure better line balancing.

The overall plan and schedule for the Bull WIP area will help to linearize the FAB line balancing. PC will maximize the moves and at the same time will look at the incoming WIP to predict the final WIP after 5 days.

Even though there is potential reduction a longer plan is required to see the potential WIP reduction at the Bull WIP area. During this time PC will work closely with Manufacturing System team to simulate the moves and also ensure the local rules dispatching system is being set to meet the PC plan moves without jeopardize the delivery.

$$TR_z = \frac{\frac{1}{m}\sum_{j=1}^{m}\sum_{i=1}^{n} Stage_i}{CycleTime_z} \quad (1)$$

$$\sum_{Proj}^{i} WIP = \sum_{curr}^{w} WIP - \sum_{di-d5}^{m} Moves + \sum_{d1-d5}^{W} WIP \quad (2)$$

$$\sum_{d1-d5}^{m} Moves = \sum_{d1}^{m} Moves += \sum_{d2}^{m} Moves += \sum_{d3}^{m} Moves += \sum_{d4}^{m} Moves += \sum_{d5}^{m} Moves \quad (3)$$

$$\sum_{d1-d5}^{W} WIP = \sum_{d1}^{W} WIP + \sum_{d2}^{W} WIP + \sum_{d3}^{W} WIP + \sum_{d4}^{W} WIP + \sum_{d5}^{W} WIP \quad (4)$$

TR = Turn Ratio
w = WIP
m = Moves
proj = projection WIP
curr = current WIP
d1-d5 = day1 to day5

1) TR calculation
2) WIP projection calculation
3) Daily Moves projection for Day1 to Day5
4) Incoming WIP projection for Day1 to Day5

Moves plan based on TR calculation. And for each of the projection in Fig 7, PC will use above formula calculation to plan and forecast moves and WIP. Moves is

Based on PC moves plan calculation, an assignable TR is being set to each stage and with the capacity allocation given to each stages. The move is planned for the Manufacturing team to meet and a layer plan moves rules also applied in the dispatching rules to govern the operators on right lots selection [20].

The rules of PC plan moves will help to maximize the moves and also repairing the line balancing by focusing additional moves requirement at a Bull WIP areas like Fig 6.It will definitely improve the factory output and delivering the WIP to downstream process is very delicate process that required a diligent planning.

In any case of BullWIP situation PC will increase the requirement of moves. Typically for 30,000 per month fab out capacity, the Salicide moves requirement is ~ 1000 moves/day. Due to the BullWIP issue, PC increase the moves requirement to 1200 moves/day anticipating that the BullWIP will be reduced in 3 weeks by having extra 200 moves more per day. Based on the incoming WIP ~ 1000 per day, the Salicide WIP will reduce to 2365. The ideal WIP for Salicide Dep stages is ~ 2200 wafers due to the multiple steps process for this stage. The Salicide Dep stage consist of 6 process steps.

At the same time to ensure the On Time Delivery intact, an assignable rules of due date has to be respected as well [21]. It must be one of the global rules in the Dispatching System that must be executed well. The layer plan will help to ensure the focus given linearly and well balancing for the resources to run each layers.

Typically a product will go through ~ 32 layers at Photolitography. Depending on the geometry of the Critical Dimensions (CD) to be printed, the Photolitography steps are mainly for Iline and DUV

scanners. The critical layers (Lower geometry < 300 nm CD) are printed at DUV. The noncritical layers will be printed at Iline (> 300 nm CD).

Looking at the capacity and requirement of moves, which typically will be aligned with the wafer loading pattern, PC team will be allocating the layers moves at each resources.

Table 1 is a typical layer plan for a multiple re-entrants process and steps at Photolitography.

This is the daily plan done by the PC team to linear the moves requirement in order to ensure the line balancing intact. A required layer plan moves is being planned by the PC based on the wafer start loading volume and it must match with the capacity. PC will set the target daily and at linear phase. There is an increment of moves requirement in any case of BullWIP situation happen. This dynamic plan have to do together with the Manufacturing System so that the Dispatching system will assign the right lots and layers. The target moves will be set in the Dispatching List. If the moves of the particular layers are met, the system will assign more lots to the next layers depending on the moves delta.

Table 2 is moves requirement monitoring done by the PC to group to ensure the average moves in a particular months are met. The dynamic activity in the wafer fabrication due to multiple pull in shipment requirement, equipment down for maintenance, WIP movement issue due to upstream constraint, BN performance issue, Customer hold etc. will cause imbalance WIP movement that may impact the daily moves plan [22]. The dynamic moves plan by PC will help to reduce the gap in any specific layers loss. At the end of each month, monitoring on the average layers moves is necessary to improve the gap loss and ensure the gap is closer.

Table 1. A typical PC layers plan for Photolitography Steps

Date	Module	IE_RESOURCE	Step	Move_req	Act_Move	Delta_move	EOH
4/28/2016	PHO	PHO-ILINE	NWell-Mask-CED	600	600	0	175
4/28/2016	PHO	PHO-ILINE	PWell-Mask-CED	600	750	150	325
4/28/2016	PHO	PHO-ILINE	HRPoly-Mask-CED	600	450	-150	100
4/28/2016	PHO	PHO-ILINE	NLDD-Thick-Mask-CED	600	1125	525	354
4/28/2016	PHO	PHO-ILINE	PLDD-Thick-Mask-CED	600	952	352	275
4/28/2016	PHO	PHO-ILINE	NSD-Mask-CED	600	871	271	300
4/28/2016	PHO	PHO-ILINE	PSD-Mask-CED	600	871	271	102
4/28/2016	PHO	PHO-ILINE	Block-Mask-CED	600	575	-25	250
4/28/2016	PHO	PHO-ILINE	MIM2_5-Cap-Mask-CED	600	575	-25	172
4/28/2016	PHO	PHO-ILINE	TopMet-Mask-CED-HS	600	827	227	411
4/28/2016	PHO	PHO-ILINE	Pad-Mask-CED	600	964	364	353

Table 2. Moves target monitoring

Target				550	600
Resource Type	**Stage**	**Step**	**FebAve**	**MarAve**	**AprAve**
I-Line	GA_NW-Mask	NWell-Mask-CED	532	579	626
I-Line	GA_PW-Mask	PWell-Mask-CED	544	573	653
I-Line	GA_HRPMsk	HRPoly-Mask-CED	501	576	555
I-Line	GA_NTKMsk	NLDD-Thick-Mask-CED	523	548	537
I-Line	GA_PTMsk	PLDD-Thick-Mask-CED	511	547	554
I-Line	GA_NSDMask	NSD-Mask-CED	490	543	581
I-Line	GA_PSDMask	PSD-Mask-CED	470	545	592
I-Line	GA_BlckMsk	Block-Mask-CED	454	550	629
I-Line	GA_M1-Mask	Met1-Mask-CED	466	569	539
I-Line	GA_V1-Mask	Via1-Mask-CED	498	562	529
I-Line	GA_MIM2Msk	MIM2_5-Cap-Mask-CED	524	520	555
I-Line	GA_V2-Mask	Via2-Mask-CED	554	493	577
I-Line	GA_M3-Mask	Met3-Mask-CED	561	510	574
I-Line	GA_TopVMsk	TopVia-Mask-CED	539	530	558
I-Line	GA_TopMMsk	TopMet-Mask-CED-HS	554	539	548
I-Line	GA_PadMask	Pad-Mask-CED	519	541	541
16		EOH	6765	5542	2712
		Total	8241	8725	9149

4. Conclusions and Summary

Developing an automated WIP Profile monitoring benefits for the PC and Manufacturing team to monitor the WIP movement real time. The nature of the process and technology in the wafer Fab that process more than 200 devices with different volume at any time, the linear start is not necessary will be a linear output. And it will also not necessary a linear line balancing. It required a close WIP monitoring and having the real time automated WIP Profile report will benefit the PC and Manufacturing team to fine tune the WIP and also the dispatching rules.

Managing the BullWIP and allocating the required output for each process especially that having multiple re-entrants process like Photolitography or Implanters are very important for Production Control team activity. They will ensure the Manufacturing team execute the right layers and step. Also not to overdo on certain steps to avoid BN starvation.

Thus having the automated WIP profile report will definitely advantages for FAB WIP monitoring. The dynamic WIP management will bring in more revenue and output for the company.

Fig. 8 shows that the BullWIP management through the automated WIP Profile management help to improve the factory utilization and also improve the output of the factory.

This paper has significantly changed the way wafer fabrication monitoring the WIP movement. There is real time monitoring that visible to the Factory Manager and the Production Control to plan the WIP movement. It is always factory goal to have a balancing WIP profile and removing BullWIP situation area.

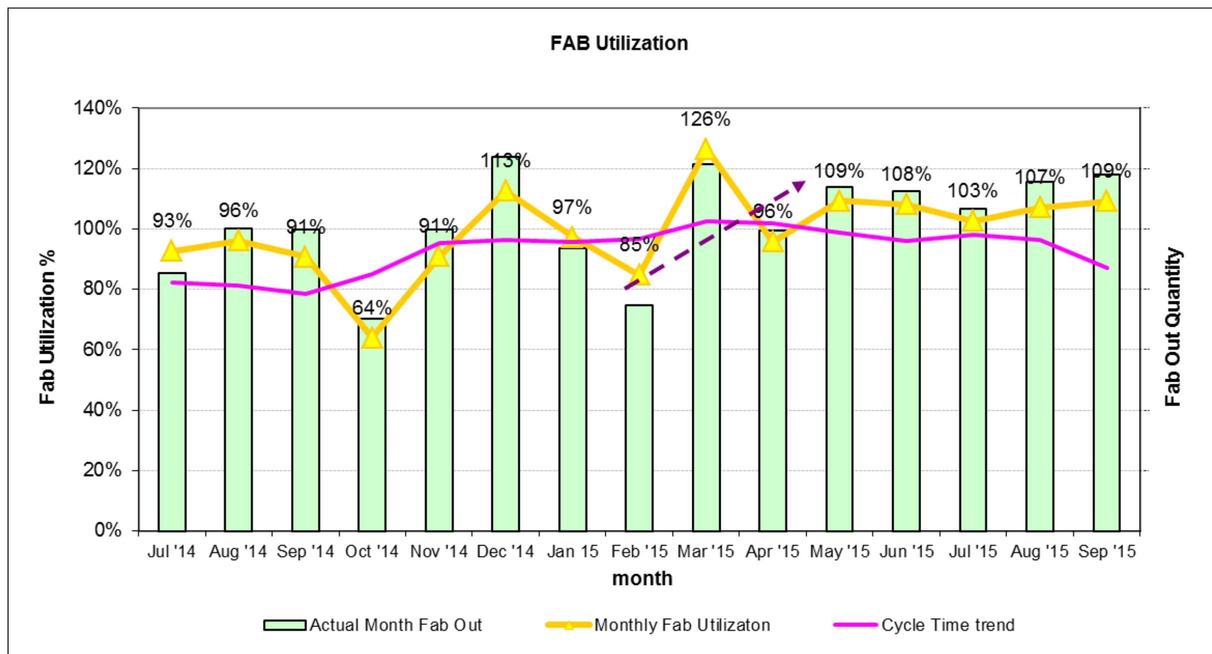


Figure 8. FAB Utilization Vs CT Vs Fab Out

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