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# High Performance Spin-Orbit-Torque (SOT) Based Non-volatile Standard Cell for Hybrid CMOS/Magnetic ICs

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**Abstract** Spin-orbit-torque magnetic tunnel junction (SOT-MTJ) is an emergent spintronics device with a promising potential. It resolves many issues encountered in the current MTJs state of the art. Although the existing Spin Transfer Torque (STT) technology is advantageous in terms of scalability and writing current, it suffers from the lack of reliability because of the common write and read path which enhances the stress on the MTJ barrier. Thanks to the three terminal architecture of the SOT-MTJ, the reliability is increased by separating the read and the write paths. Moreover, SOT-induced magnetization switching is symmetrical and very fast. Thus, doors are opened for non-volatile and ultra-fast Integrated Circuits (ICs). In this paper, we present the architecture of a mixed CMOS/Magnetic non-volatile flip-flop (NVFF). We use a compact model of the SOT device developed in Verilog-A language to electrically simulate its behaviour and evaluate its performances. The designed standard cell offers the possibility to use the usual CMOS flip-flop functionality. In addition, it enables storing and restoring the magnetic data by exploiting the non-volatility asset of MTJs when the circuit is powered off. With a 28nm dimension, the SOT-MTJ based NVFF demonstrated a very high speed switching (hundreds of picoseconds) with 7× decrease in term of writing energy when compared to the STT device.

**Keywords** Spin Orbit Torque, Compact Modeling, Verilog-A, Simulation, Spin Transfer Torque, MRAM, Flip-flops, Spintronics

## 1. Introduction

Technology innovations are mainly motivated by the worldwide tenders around them. Portable computing and connectivity have a continuous market demand. Thus, various technology advances for smartphones, tablets and wireless devices have seen the light. Nowadays, mobile systems are dominating the semiconductor market. However, one keystone of mobile systems is their power autonomy. For battery-powered applications, energy efficiency is a critical figure of excellence. The great challenge which is facing semiconductor big companies is to provide low power consumption products while improving their performance. In addition, the size of electronic devices has become an attractive standard for the customer. Thus, Integrated Circuits (ICs) are becoming denser.

For four decades, the semiconductor industry has succeeded to follow Moore's law by doubling the performance and the number of transistors in silicon dies area every 18 months. Nevertheless, the last decade, the limits of conventional device scaling are fronting major problems, such as leakage current, performance saturation, acute device variability and process complexity.

Trying to overcome these hurdles, several solutions are studied at technology, circuit and architecture levels. The use of non-volatile devices is appreciated as a promising solution to reduce power consumption, increase data storage safety and offer new functionalities. Several technologies are intensively inspected, for instance, Phase Change Random Access Memory (PCRAM), Ferroelectric RAM (FeRAM), Redox RAM and Magnetic RAM (MRAM). In its 2010 report [1], ITRS identified Redox RAM and MRAM as the two most favourable technologies for embedded memories at advanced technology nodes.

MRAMs exist thanks to the discovery of the Magnetic Tunnel Junction (MTJ) in 1995 [2]. Since then, four main generations of MRAMs have seen the light. The first generation of NV MRAM is magnetic-field controlled known as Field Induced Magnetic Switching (FIMS) [3]. This approach suffers from selectivity and scalability issues.

The selectivity issues were partially solved by the so-called "toggle" approach proposed in [4], but field-based writing schemes remain hardly scalable below 90nm. Then, came the Thermally Assisted Switching (TAS), which allowed solving the selectivity issues while reducing the writing energy and improve the scalability [5]. A high writing current is required and consequently increased power consumption and die area due to large transistors and huge write lines. Further, more advanced writing scheme has been proposed to solve the latter issues; spin polarized current can be used through the junction to apply spin transfer torque (STT) [6] and switch the magnetization of the storage layer. Although the writing current has been decreased by orders of magnitude and the scalability issue is improved, two main shortcomings are still limiting the reliability and endurance of STT-MRAMs; i) the writing current stress can occasionally damage the MTJ barrier, ii) a read operation can undesirably switch the MTJ magnetization state.

Recently, in [8-12] it has been proved that such an issue could be avoided by the demonstration of Spin-Orbit-Torques in ferromagnetic thin films. In this work, we report the benefits brought by the SOT device to increase the reliability and performances of MTJ based ICs focusing on a NV flip-flop study case. To do so, we also introduce a macrospin compact model that we developed in Verilog-A language to describe the behaviour of the SOT-MTJ device and enable its integration into semiconductor commercial design flows to realize hybrid CMOS/magnetic ICs. Simulations results show the great potential of SOT-MTJ to improve the writing energy compared with STT-MTJs for a non-volatile flip-flop (NVFF) study case. Results are very encouraging for future complex hybrid magnetic/CMOS systems targeting Application Specific Integrated Circuits (ASICs) and memories.

Section 2 introduces the structure of the SOT-MTJ as well as the compact model used to integrate the device in the CMOS design flow. In section 3, we describe the architecture of the CMOS/magnetic NV flip-flop validated by simulations results. In section 4, we evaluate the performance metrics of the designed cell and we discuss them. Section 5 is the conclusion.

## 2. SOT-MTJ: Structure and Modeling

Magnetic Tunnel Junction (MTJ) is used as the basic memory elements in MRAM cells and magnetic logic devices. The MTJ is a nanostructure composed of two ferromagnetic layers (FM) such as cobalt, iron, or nickel separated by a thin layer of insulator typically alumina oxide or magnesium oxide which represents the tunnel barrier. The first FM layer (hard layer) -with a pinned magnetization- acts as a reference while the second FM layer (soft/free layer) -with a free magnetization- acts as a storage layer. The magnetization of the storage layer can be switched between two stable states, either parallel (*P*) or antiparallel (*AP*) with respect to the reference layer. In other words, considering that the spins of the reference layer are always "up", if the spins of the storage layer are also "up" (in the same direction of the reference layer) so the resistance of the MTJ is "low" (*Rp*) and we call this as parallel "*P*" state. If the spins of the storage layer are "down" (in the opposite direction of the reference layer), we call this as antiparallel "*AP*" state and the resistance of the MTJ is "high" (*Rap*), as shown in figure 1 (c). These two configurations can be used to code two different logic states; logical 0 (low resistance) and 1 (high resistance). This resistance variation behavior was first observed and explained by Jullière [13]. Tunneling magnetoresistance ratio (*TMR*) describes the ratio between the two resistance values as expressed by the equation

$$TMR = \frac{R_{AP} - R_P}{R_P}$$

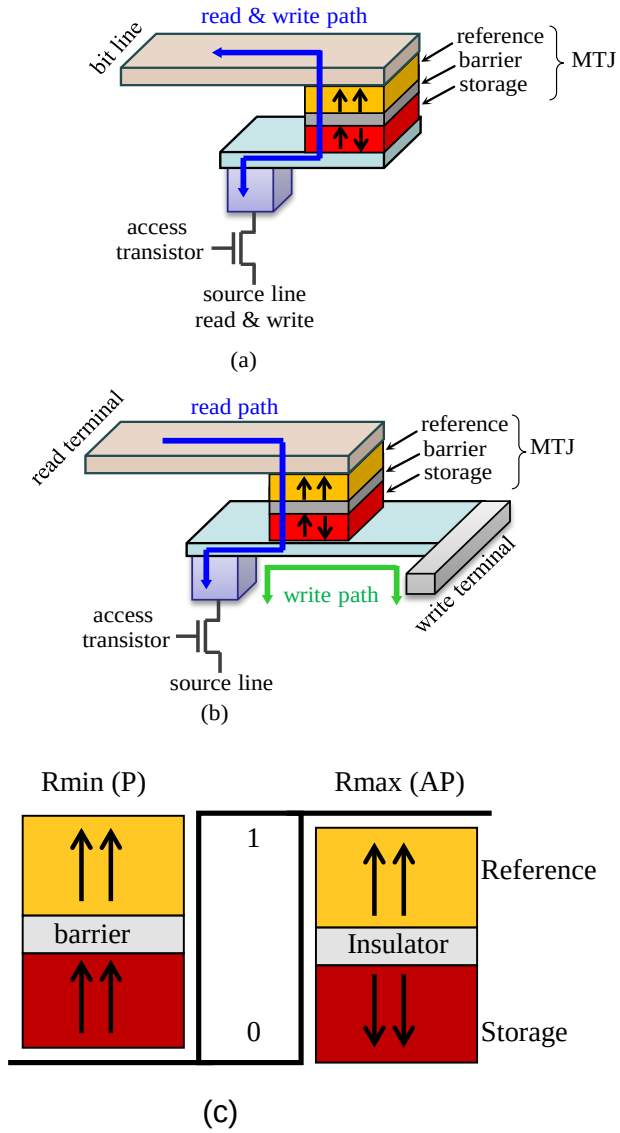


**Figure 1.** Comparison of MTJ based standard bit-cell (a) STT-MTJ based bit-cell (b) SOT-MTJ based bit-cell, In-plane current injection through the write line induces the perpendicular switching of the storage layer (up or down) (c) Resistance variation of the MTJ according to the storage layer magnetization state

For the 2-terminal STT device shown in figure 1(a), both read and write operations are achieved by passing a current through the junction. Figure 1 (b) shows the 3-terminal structure of the SOT device with independent read and write paths. The magnetic free layer is in contact with a nonmagnetic heavy metal stripe, typically platinum (Pt) or Tantalum (Ta) [8-12]. When injecting a current in the nonmagnetic layer, spin-orbit coupling leads to a perpendicular spin current induced by the spin Hall and Rashba-like effects which is transferred to the magnetization creating a spin torque and inducing magnetization reversal [8-12].

The development of a compact model for electrical simulations is a necessary step to integrate exotic devices such as the SOT-MTJ in industrial CMOS design flows. In general, two approaches are used in literature to model MTJs. The first is mainly based on physical equations known as "the Landau-Lifshitz-Gilbert (LLG) Equations" [14], the second is more behavioral to fit characterization results [6], it is so called 'analytic" approach. It is the linearization of the LLG approach at switching points. The first approach describes the behavior of the device more realistically and is generally more generic and flexible. The second one is simpler in implementation but less generic and more adequate for a given technology since parameters can be adapted to experimental data. Compact models can be implemented using a generic language like C and compiled for a given simulator, or using a generic language such as Verilog-A.

In order to simulate the switching behavior of the SOT-MTJ, we developed a compact model written in Verilog-A language which is on the path to becoming the preferred compact modeling language for both academic and industrial research groups. The modeling approach used for the SOT device is based on macrospin approximations. It describes the SOT-MTJ as a three-terminal logic device and includes the dynamic behavior described by the LLG equations. The model uses a set of mathematical equations, physical considerations as well as many technological parameters. In [15-17], a full description with the study of different operating modes and parameters variation effects has been explained in details.

Figure 2 shows the simulation results of the SOT-MTJ compact model based in [15-17]. The model behavior faithfully corresponds to the theoretical switching of the magnetization Mz from parallel '*P*' to '*AP*' and vice versa depending on the current direction applied during the time. Since the model is dynamic and accurate, we clearly observe the oscillations during the switching (write phase). In addition to the fast speed switching, we clearly observe in figure 2 that the switching time from a state to another is the same. Thus, this natural symmetry offered by the SOT switching eases the design task at circuit level.

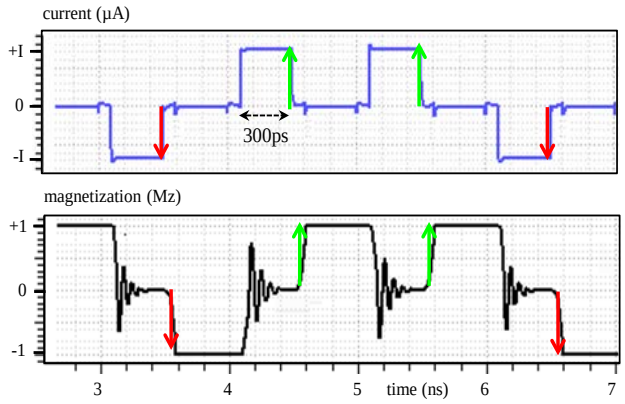


**Figure 2.** Validation of the SOT-MTJ Verilog-A compact model through electrical simulations

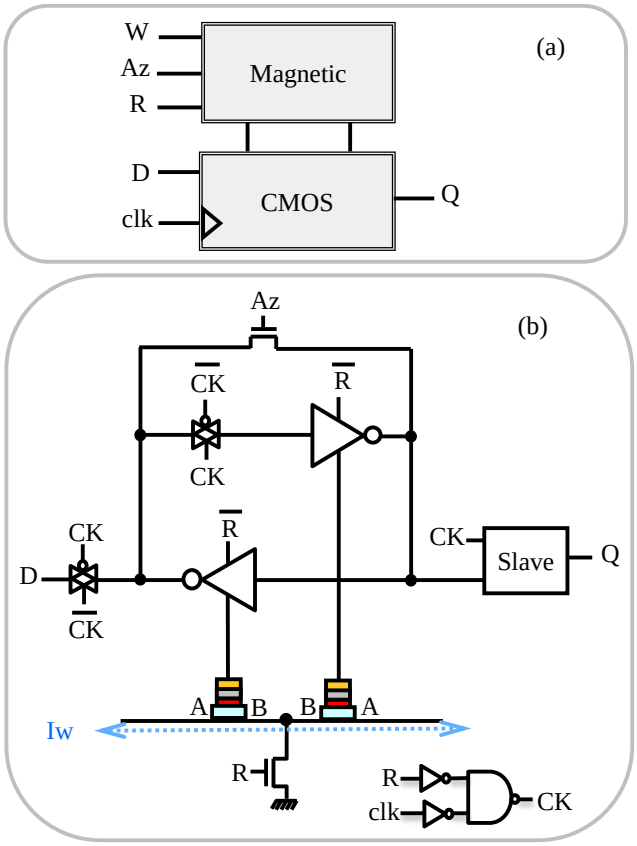


**Figure 3.** SOT based NVFF (a) Symbol of the NVFF with the corresponding inputs and outputs (b) Detailed architecture

## 3. SOT Based NV Flip-Flop (NVFF) Architecture

The architecture of the NVFF meticulously relies to the typical CMOS flip-flop circuitry as shown in figure 3. The integration of the magnetic part is carefully accomplished with an optimized way to not disturb the CMOS operation while requiring the minimum number of transistors. Thus, non-volatility is obtained while keeping the advantage of working under the usual CMOS mode and so profit from the high performance of silicon.

Two operating modes are available:

i) CMOS operating mode: when *R='0'*, the magnetic part of the NVFF is disconnected from the rest of the circuit. The NVFF takes the signal '*D*' as an input and the behaviour of the cell is purely CMOS. Thus, the performance of the silicon is fully exploited. During this phase, it is possible to write the two junctions in a differential way since the reading operation is also differential meaning that the two MTJs have an opposite configuration state (*P* and *AP*). We inject a writing current, *'Iw'* through the common writing stripe of the two junctions. The current flows from *A* to *B* for the 1st device and from *B* to *A* for the 2nd device. Thus, the magnetization state is *Mz= 1* for the first junction and *Mz= -1* for the second, or vice-versa.

ii) Magnetic mode: When R ='*1*', the input signal '*D*' is disconnected from the rest of circuit since the input pass-gate is switched off by '*CK*'. At first, the '*Az*' signal is set to '*1*' during a very short time (few picoseconds) to establish an electrical equipotential. When '*Az*' is deactivated, the cell behaves as a sense amplifier and restores the magnetic data from the two different resistances of junctions.

Figure 4 illustrates the two possible NVFF modes. During the CMOS mode, the appliance of a positive current pulse *Iw* writes the '*1*' data by setting the magnetization *Mz* of the two MTJs up *(+1)* and down *(-1)*, respectively. The opposite data *'0'* is obtained when *Iw* is negative. The output *Q* of the NVFF takes the value of the input data *D* at each rising edge of the clock *CK*. This corresponds to the standard CMOS operating mode. The CMOS mode is interrupted when *R='1'* and the magnetic data already written in the MTJs is restored. Figure 4 shows that during the first restore operation, the output Q recuperates the '*1*' data stored as magnetic state *Mz*. Then, during the second restore, the '*0*' data is loaded back. Figure 4 confirms the non-volatility criteria of the NVFF, where the last data stored in the MTJs is loaded back after a power-off of the cell.

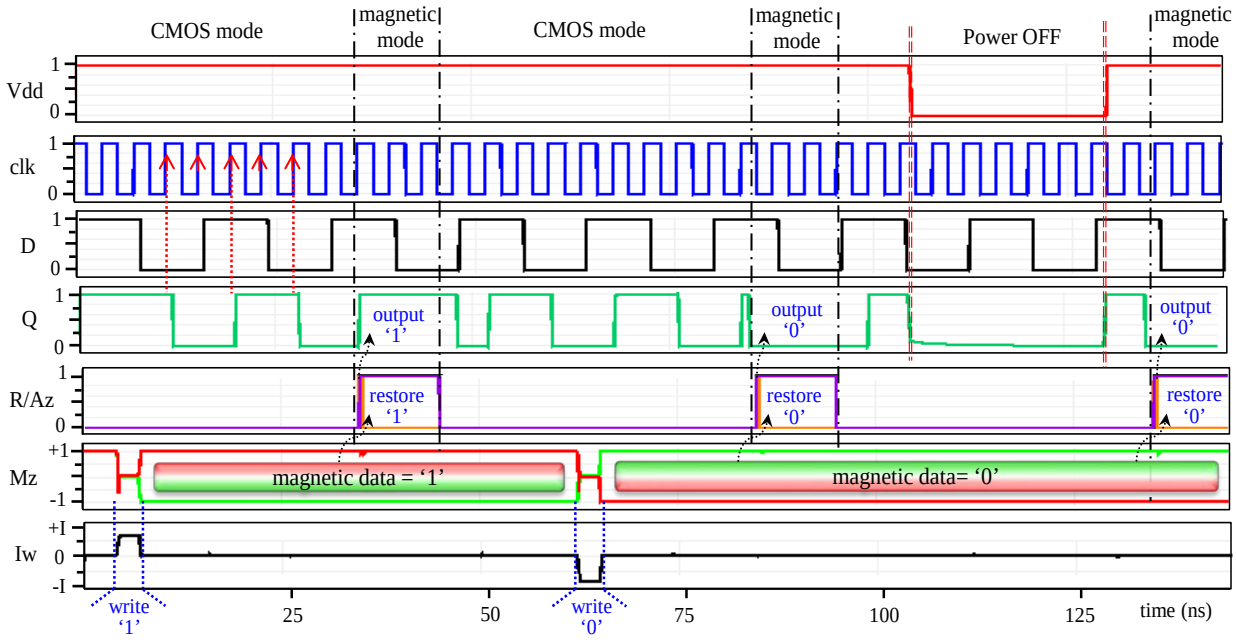


**Figure 4.** Transient simulations of CMOS/magnetic mixed NVFF. Two operating modes are possible: CMOS and magnetic modes. During the CMOS mode, the output 'Q' of the NVFF follows the input data 'D' at every rising clock 'clk' edge. During the magnetic mode, we proceed to a read operation by enabling 'Az' and 'R' signals, the output 'Q' corresponds to the '1' or '0' state stored as magnetic data. ***Vdd***: supply voltage, ***D***: input data, ***clk***: clock signal, ***Q***: NVFF output, ***R***: restore signal, ***Az***: auto-zero signal (potential equalizer), ***Mz***: magnetization state, ***Iw***: writing current

## 4. Performance Analysis

The resistance of the MTJ (*Rp, Rap*) is a critical restriction that marks both read and write operations. For a reliable read operation, it is desirable to have suitably high resistance. This is mainly due to the access transistors connected to MTJ which decrease the effective TMR by adding a series resistance. If the MTJ resistance is reasonably greater than that of the transistor, the influence of series resistance is less significant. Commonly, the control of the MTJ resistance is achieved by adjusting the MgO barrier thickness which also enhances the Tunneling-Magneto-Resistance (TMR). Nevertheless, for a write operation, high resistance is not desirable, because it worsens the source deterioration effect and limits driving current from the transistor. Defining an optimal resistance window that allows both high-speed read and write operations is the bottleneck of the STT technology. This dilemma seems to be removed thanks to the three terminals architecture of the SOT-based bit-cell, for which the read path and the write path are separated.

Based on the current state of the art of MTJ devices, we drive a comparison study in terms of writing current and energy. Since the interest of MTJs is greater at advanced technology nodes and also in order to be more faithful to the macrospin assumptions used in the macro-model, we investigate the SOT and STT devices at 28 nm dimension. We target a fast switching of 1ns.

As shown in figure 5, for a given applied voltage, the very low resistance of the write path offers the possibility to attain a high write current. When associated to the semi-processional switching nature of SOT devices [8-12], ultrafast speed can be attained. Experimental results of the SOT device show that it is possible to switch at only 380ps [11] [17]. Also, theoretical predictive studies of the SOT technology as well as results from our model proclaim that the SOT device can perform at few hundreds of picoseconds [7] [18-21].

Benefits in terms of energy per writing operation can also be observed since the writing stripe is highly conductive (Pt), the writing path has a very low resistance ($R_{Pt}$). If we consider Ic the critical writing current, $R_w$ the resistance of the writing path and $\tau$ =1ns the width of the writing pulse, the energy can be calculated as ($E= R_w \times Ic^2 \times \tau$). In MTJ based NVFFs, we are writing two junctions in the same time for a differential read operation. Therefore, the writing path resistance is further increased and so the required energy. Table 1 shows the values of the critical current required for each technology as well as the writing energy for the given devices parameters. Although the critical current of the SOT-MTJ is higher than that of the STT-MTJ, the required energy per writing operation of the SOT technology is still 7× better than its STT counterpart. This is due to the low writing path resistance of the SOT-MTJ.

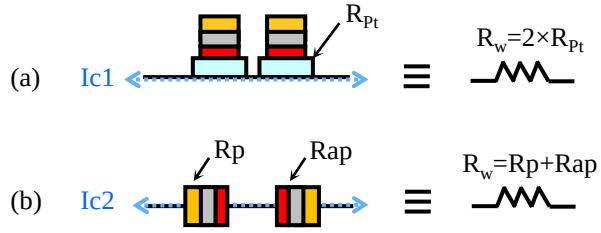


**Figure 5.** Equivalent resistance of the writing path (a) SOT device (b) STT device

**Table 1.** SOT versus STT parameters and performance

| Technological parameters | SOT | STT |
|---|---|---|
| Storage layer volume ($nm^3$) | 28×28×0.6 | $\pi\times(28^2/4)\times1.69$ |
| Write stripe dimensions (nm) (length, width, thickness) | (45, 28, 2) | - |
| Write stripe resistivity μΩ.cm (Pt, Ta, W) [7] | (20, 190, 180) | - |
| Sat. magnetization ,Ms (A/m) | $1.1\times10^6$ | $1.1\times10^6$ |
| Damping factor, α [7] | 0.5 | 0.008 |
| Spin Hall angle (Pt, Ta, W), $\Theta_{SHE}$ [7] | (0.07, -0.15, 0.3) | - |
| Bias magnetic field (mT) [7] | 30-100 | - |
| Parallel resistance Rp (KΩ), RA @ (0V,300K) = 5.8 Ω.μm² | 9 | 9 |
| $Tmr_0$ @ (0V, 300K) | 70% | 70% |
| Jc ($A/m^2$) @ 1ns [7] | $2.6\times10^{12}$ | $7\times10^{10}$(P→AP)<br>$4.9\times10^{10}$(AP→P) |
| Ic (μA) @ 1ns | 140 | 43 (P→AP)<br>30 (AP→P) |
| Write path resistance of 1 MTJ (KΩ) | 0.160 (Pt) | ~ 9 (Rp)<br>~ 16.4 (Rap) |
| Writing energy (fJ) @ 1ns | 6.28 | 44.8 |

## 5. Conclusions

Memory and logic design communities are interested in the integration of MTJs with CMOS circuits. The SOT-MTJ device is becoming a hot topic in both academic and industrial R&D. We proposed the use of such a device in the case of a NVFF standard cell which can be used as a primitive cell into design kit libraries offering safety, power reduction and instant on/off. In addition the increased reliability due to its three terminal structures, simulations results based on an accurate compact model showed the great potential of SOT-MTJ to improve the writing energy by 7× compared with STT-MTJs. Also, a very fast switching (hundreds of picoseconds) has been observed.

Results are very reassuring for future complex hybrid magnetic/CMOS system. Also, the intrinsic hardness to radiation of MTJs is a very interesting asset for aerospace and military applications.

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