

Investigation of Digital Signal Processing of High-speed DACs Signals for Settling Time Testing

Rokas Kvedaras¹, Vygaudas Kvedaras¹, Tomas Ustinavičius^{1,*}, Audronė Kvedarienė²,
Ričardas Masiulionis¹

¹Faculty of Electronics, Vilnius Gediminas Technical University, Lithuania

²Faculty of Business Management, Vilnius Gediminas Technical University, Lithuania

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Abstract Filtering of the measurement signals using digital brick-wall comb filters in frequency domain developed by the authors and measurement of the settling times of DACs are discussed in this paper. Results of the investigations made have shown that digital brick-wall comb filters are capable of reducing noise level by 10 times while keeping measurement signal undistorted. Investigation of the developed settling time measurement algorithm has determined influence of the internal noise of the sampling converter, noise of the transmission line, ADC and other sources of noise to the settling time measurement errors. It has been proved that by using the earlier developed measurement converter and the proposed digital filtering of the DAC signal it is possible to measure settling times of 12-14 bit DACs.

Keywords Digital Signal Processing, Digital Brick-wall Comb Filter, Settling Time Measurement, DAC Settling Time

1. Introduction

High-Speed digital-to-analogue converters (DACs) are widely used in today's electronics industry. Settling time of the DAC output signal is one of the most important parameters characterizing the speed of DAC in use [1, 2]. Settling time of modern 12–16 bit High-Speed DAC is in range of tens of nanoseconds. Settling time has to be measured according to the resolution of the DAC itself and for 14 bit DAC the threshold voltages of the settling time measurement is only $\pm 1/(2^{15})$ (0.5 of Least Significant Bit (LSB)) of maximum output voltage. Therefore it is rather complex task to measure this parameter during DAC pre-manufacturing and manufacturing process [1–7].

The topic is not widely investigated and some authors [2, 6, 7] are proposing measurement techniques for 18 bit DACs with settling times up to 30 ns. The proposed methods are

using oscilloscope as a measuring device and are based on specialized sampling converters to secure wideband oscilloscopes from being overloaded. The main disadvantage of such method is that settling times are measured on the screen of the oscilloscope and therefore it is not automated and requires a very high-skilled operator.

The automated sampling testers were developed and implemented by the authors. These testers are suitable for measurement of settling times of High-Speed 8–14 bit DACs [4, 5, 8]. Specialized precise circuits of sampling time step shaping, inverse timescale conversion method, compensating low-noise sampling heads [4, 10], and methods of amplitude normalization and automatic measurement of settling times were developed and successfully implemented for these testers. In order to perform automatic measurement of settling times of 14 or higher resolution DAC it is necessary to convert DAC output signal with transformed timescale to digital form and to perform digital signal processing [4, 8].

For this purpose tester with conversion of output signal and the developed digital processing has been developed and implemented [10]. Implementation of a digital signal processing (DSP) of measurement signal has enabled further reduction of influence of internal noise of sampling head and therefore increased measurement accuracy. Further investigations of the developed testers and DSP algorithm have shown that it is possible to use these testers for settling time measurement of 12–14 bit high-speed DACs with readout levels of 0.5 LSB (for 14 bit DACs — 0.003%) while most of the IC producers are providing settling time measurement results on 0.1% — 0.025% level of full scale for high-speed DACs in production. Authors have developed and investigated a new structure of the sampling tester for measurement of dynamic parameters of high-speed DACs [11] using best achievements of the previous testers and extending their capabilities by the use of modern components and digital signal processing algorithms. In the paper [8] new principles of digital signal processing including the implementation of the newly designed comb

filter and complex processing using comb filter and averaging of the arrays of the filtered signals has been proposed. The initial investigations have shown that the complex signal processing method ensures the reduction of the $1/f$ noise and white noise by 100 times. Nevertheless there were no detailed investigations made on how it affects the measurement accuracy of the settling time.

The aim of this paper is to present new results of investigation of DSP for settling time determinations applying the proposed comb filters.

2. Digital Filtering of Measurement Signal

As it has been stated earlier the readout threshold voltage levels are very small (Fig. 1). Therefore the internal noise of the sampling converter has the essential role on the errors of measurement of settling time. Accordingly, the developed digital signal processing algorithm to be developed should be capable to eliminate noise in the specified frequency range but at the same time it should not influence the test signal anyhow. Because of the small threshold levels the requirement not to influence the test signal itself is very important as insignificant changes of the measurement signal can change measurement results dramatically.

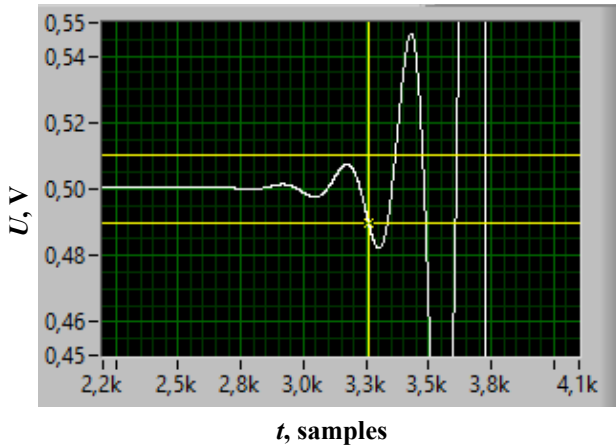


Figure 1. View on the measurement signal model in LabView®. Time difference between two samples is 0.2 ns taking into account time scale transformation in sampling converter

This means that the pass-band characteristic of the filter has to be absolutely flat. Even fractional distortions of test signal itself would make measurements of the settling time impossible.

2.1. Digital brick-wall Comb Filter

In the proposed converters [10], the measurement signal from the sampling converter is converted to a digital form using ADC and the digital signal is loaded to the personal computer (or any other digital processing unit). Regarding the controlled manner of the measurement (each

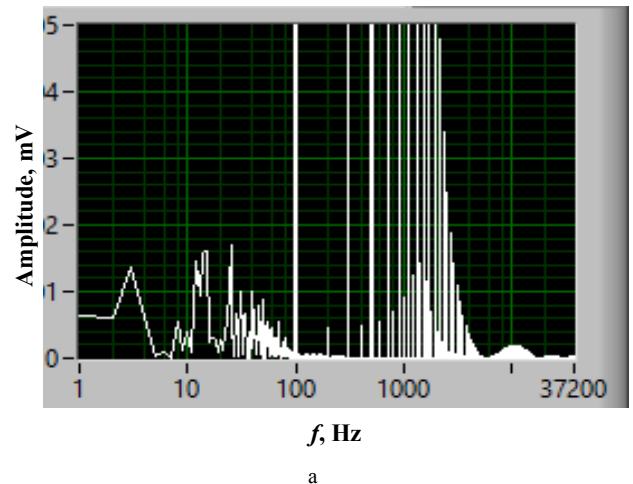
measurement is initiated by the control software or manually by the operator) it is possible to obtain full measurement signal without application of special windows that are normally applied for the digital processing of the continuous signals. The resulting digital array of the measurement signal can be cut so that there is only the required part (e.g. one single period) of that signal is left. It is proposed to append n_r arrays of single periods of different realizations of a measurement signal (obtained from n_r measurements) to the continuous uniform signal of periodic test pulses and to obtain pseudo-periodic test signal this way. As the period of the measurement signals with converted timescale in such appended array is known and number of the measurements that were appended in the array is set then by using a test signal with a converted timescale as a clock signal for ADC it is possible to achieve that the spectrum of such pseudo-periodic array is discrete and concentrated in certain periodic harmonic components and does not have extra spectrum components at the side of main harmonics. By digitalization and recording of n_r realizations of test signal forming pseudo-periodic series of test signals to the PC memory, internal noise of sampling head, noise of transmission line, ADC and other components are digitized together.

The resulting array of the pseudo-periodic test signal with $1/f$ noise white noise and other influencing noise components are converted to the frequency domain using FFT (Fig. 2a). Figure displays that the spectrum of the most components of noise (that are not periodic in general) can be clearly distinguished from the discrete spectrum of the test signal.

The resulting spectrum is filtered by using a developed digital comb filter. The investigations convince that the best results are obtained by using a comb filter with the following characteristics [8]:

$$H(f) = \begin{cases} 1, & \text{when } f = mf_0 \\ 0, & \text{elsewhere} \end{cases}, \quad (1)$$

where f_0 – main harmonic of the test signal; $m = 1, 2, 3, \dots$



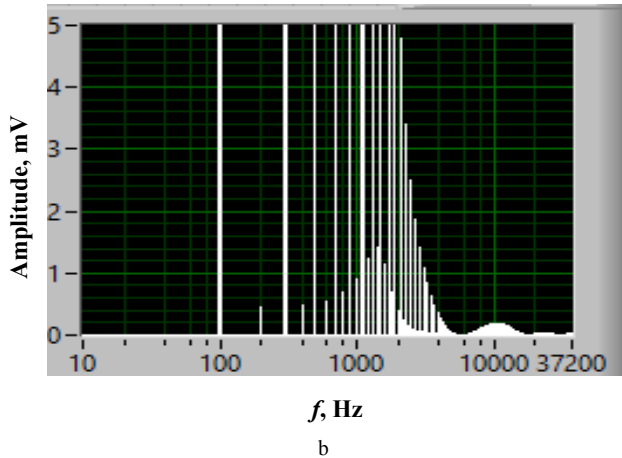


Figure 2. Magnitude spectrum of pseudo-periodic test signal and internal noise (a) and magnitude spectrum of brick-wall comb filter output (b).

After this filter all the spectral components of noise differing from the main test signal spectral components (mf_0) are blocked (set to $m_i = 0+0j$ values). Therefore major spectral components of the noise, those whose frequencies are not equal to the frequencies of the test signal, are eliminated from the resulting spectrum (Fig. 2b). The resulting spectrum is converted back to the time domain by using an inverse FFT. After filtering in frequency domain and inverse FFT the infinite periodic sequence of the filtered signal is obtained as an output. All periods of this signal and noise are equal. It is obvious that such filtering can be implemented only in case spectrum of the test signal is finite. Spectrum of output signal of the compensating sampling converter is finite as the passband is limited by elements of the converter and the Nyquist frequency of ADC.

The investigation of the developed digital comb filter and settling time measurement has been tested applying LabView® software.

2.2. Digital model of DAC Output Signal

The measurement signal in LabView® has been modeled using sum of two signals: a square signal and harmonic settling signal. The model of an ideal measurement signal has been expressed as:

$$u(t) = U_S - a_S e^{-b_S(t_G - t)} \sin[c_S(t_G - t) + d_S], \quad (2)$$

where t_G – duration of the flat part of the DAC output pulse, a_S , b_S , c_S , d_S – approximation parameters of the output signal.

Model of the ideal measurement signal is provided in Fig. 1.

Noise components were simulated by (a) using sine wave of f_{n1} frequency, and initial phase of which for each test signal realization is set randomly by using continuous uniform distribution from 0 to $\pm 360^\circ$ and (b) standard white noise. The noise signal is added to the ideal test signal realization. Model of the measurement signal with noise is shown in Fig. 3.

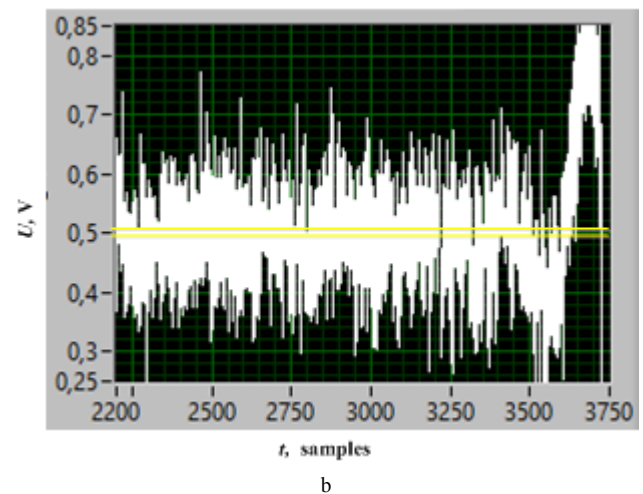
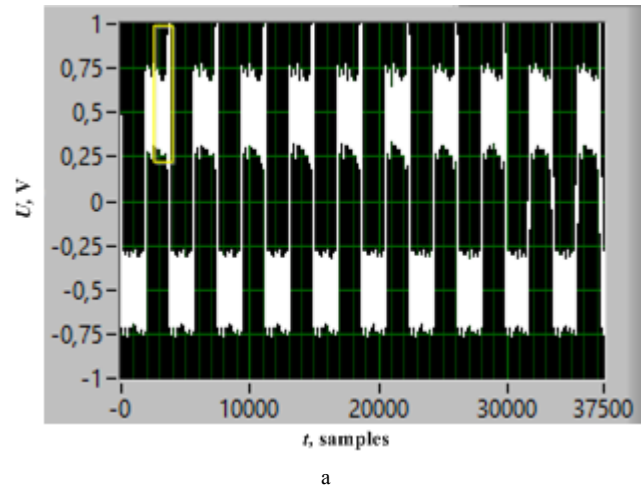


Figure 3. The view on the LabView® model of test signal with noise in different scale.

It is obvious that with the given readout threshold voltage levels (shown as yellow horizontal lines in Fig. 3b) and noise of the converted signal measurement of the settling time is not possible.

2.3. Investigation of Noise Suppression

Operation of the filter has been investigated at first. Pseudo-periodic array of undistorted (ideal) test signal has been filtered by the developed brick-wall comb filter. Discrete values of the resulting array of the filtered signal have been subtracted from the corresponding values of the array of the initial test signal. The result of the subtraction was an array of zero values which means that the filter developed is not distorting the measurement signal itself and does not affect result of settling time measurement.

Effectiveness of the filtering of the model of the real test signal has been investigated. The pseudo-periodic test signal array was formed using from 2 to 100 different signal realizations during the investigations. Spectrum of the pseudo-periodic test signal is shown in Fig. 2a. Signal noise

is set to standard deviation $\sigma = 0.3$ V. The measurement signal in frequency domain is filtered by the developed comb filter (1) implemented in LabView®. Analysis of the spectrum of the filtered digital test signal with noise has shown that spectral components of the noise signal are absent. Inverse FFT performed on the resulting spectrum to get test signal after filtering in the time domain. Filter input noise (unfiltered) is shown in Fig. 3 and filter output (filtered) signal is shown in Fig. 4. It is important to note that the developed digital filter has not influenced the testing signal and the error generated by the internal noise has reduced significantly. The yellow horizontal lines represents settling time readout levels and the vertical yellow line is the beginning of the settling time measurement.

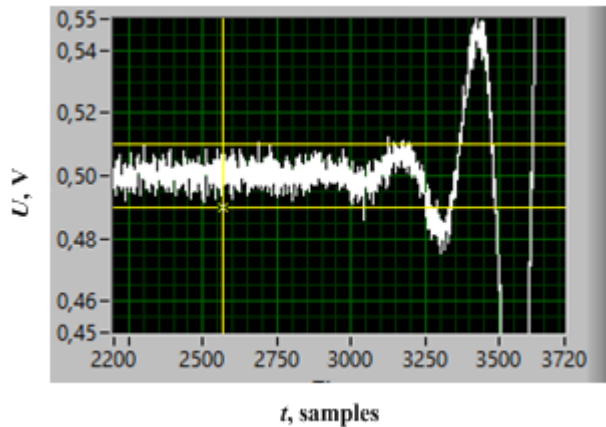


Figure 4. The filtered signal representation in time domain

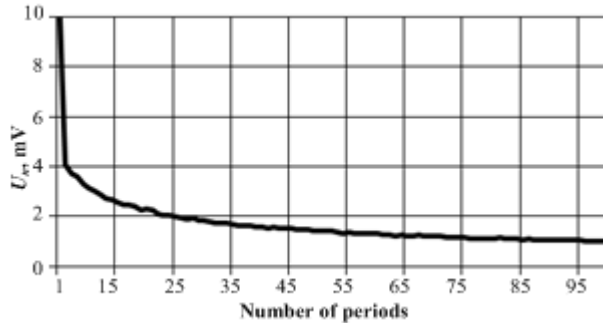


Figure 5. Intensity (peak-to-peak) of a white noise on an output of the digital brick-wall comb filter when intensity (peak-to-peak) of a white noise in input is ± 10 mV

Fig. 5 represents intensity of a white noise on an input and an output of the digital brick-wall comb filter while using different number of periods for forming pseudo-periodic signal. It is seen that by the increase of number of periods effectiveness of the filtering is increasing rapidly (5 times) in initial stages (up to 25 periods) and noise level is reduced by 8 mV. Increasing number of periods further on is not resulting in such effective reduction of noise: changing number of periods from 75 to 95 the noise level is reduced only by 0.1 mV. Therefore the optimum performance is gained by using 65 – 85 realizations of the measurement signal to form pseudo-periodic array. In order to obtain best

filtering effectiveness 100 signal realizations shall be used to form measurement signal for further investigations.

In order to investigate effectiveness of the filtering of the test signal to the settling time measurement accuracy digital settling time measurement algorithm has been developed and implemented.

Digital array of the test signal with noise is filtered using the comb filter then magnitude of the test signal is normalized and readout (threshold) levels are set according to the resolution of the DAC under test. In order to calculate settling time each discrete value of the test signal array is compared to the threshold levels starting from the trailing edge of the signal. In case a discrete value of the signal is higher than the upper threshold level or lower than lower threshold level the number of the discrete value in the array is recorded as settling time measurement value. This value can be transformed to the settling time value by taking into discretization frequency and time transformation value of the sampling converter. In case an array of the test signal without noise is fed to the settling time calculation algorithm – an ideal settling time value for this particular test signal is calculated. Difference of the ideal settling time value and the value calculated for the test signal with noise multiplied by length of one discrete and divided by time transformation coefficient is an absolute measurement error.

3. Investigation of Influence of Digital Filtering Algorithm to the Accuracy of Measurement of Settling Time

The different types and models of DACs leads to different process of settling of the output signal meaning different maximum magnitude and decrement of the ringing. In order to investigate effectiveness of the filtering to the measurement of settling time for different conditions the decrement of the ringing of the test signal has been set to $b_S = 45, 70$ and 140 . Investigations have been made using $n_r = 100$ realizations of the test signal. The magnitude of the standard deviation of the white noise has been changed during the investigations to obtain a ratio of noise level to the readout levels is acceptable for settling time measurements. The results of settling time measurement investigation using readout levels of 0.5 LSB (± 61 μ V) of 13-bit DAC is provided in Fig. 6 a. It is seen that with ringing decrements of $b_S = 70$ and 140 , standard deviation of white noise up to 0.8 of readout levels settling time measurement error is $\leq (+1.2; -0.4)$ ns. The proposed converters [10] have standard deviation of noise $\sigma_n \leq 35$ μ V (ratio $\sigma_n/U_I = 0.54$) error of the settling time measurement is $\leq \pm 0.4$ ns (meaning $\pm 2\%$ with DAC settling time of 20 ns). In case the test signal has long decrement of settling ringing ($b_S = 45$) the highest magnitude value of one of the periods gets very close to the readout levels and thus measurement errors increase rapidly (even small amount of residual noise after filtering makes some of discrete values near the highest magnitude value to exceed

threshold value). The investigation results for 14-bit DAC with the readout levels of 0.5 LSB ($\pm 30 \mu\text{V}$) are provided in Fig. 6b. It is seen that settling time measurement error is $\leq (+1.4 -0.6)$ ns (with $b_S = 45$) with the ratio of standard noise magnitude deviation to the readout levels is $\sigma_h/U_l \leq 0.92$. Thus, the proposed converters can't be used with standard noise magnitude deviation of $\sigma_h \leq 35 \mu\text{V}$ (ratio $\sigma_h/U_l = 1.1$). It is necessary to reduce standard deviation of noise magnitude of the converter at least to the level $\sigma_h \leq 17 \mu\text{V}$ (ratio $\sigma_h/U_l = 0.56$). In this case settling time measurement error is ± 0.4 ns ($\pm 2\%$, in case settling time of the DAC

under test is 20 ns).

It is obvious that using the proposed digital brick-wall comb filter in frequency domain it is possible to measure settling times of the 13 bit DACs with readout levels of 0.5 LSB. In order to measure settling times of 14 bit DACs it is necessary to use sampling converters with standard deviation of noise magnitude less than $20 \mu\text{V}$. In order to measure settling times of the DACs with higher resolution it is necessary to make further improvements to the algorithm of digital signal processing.

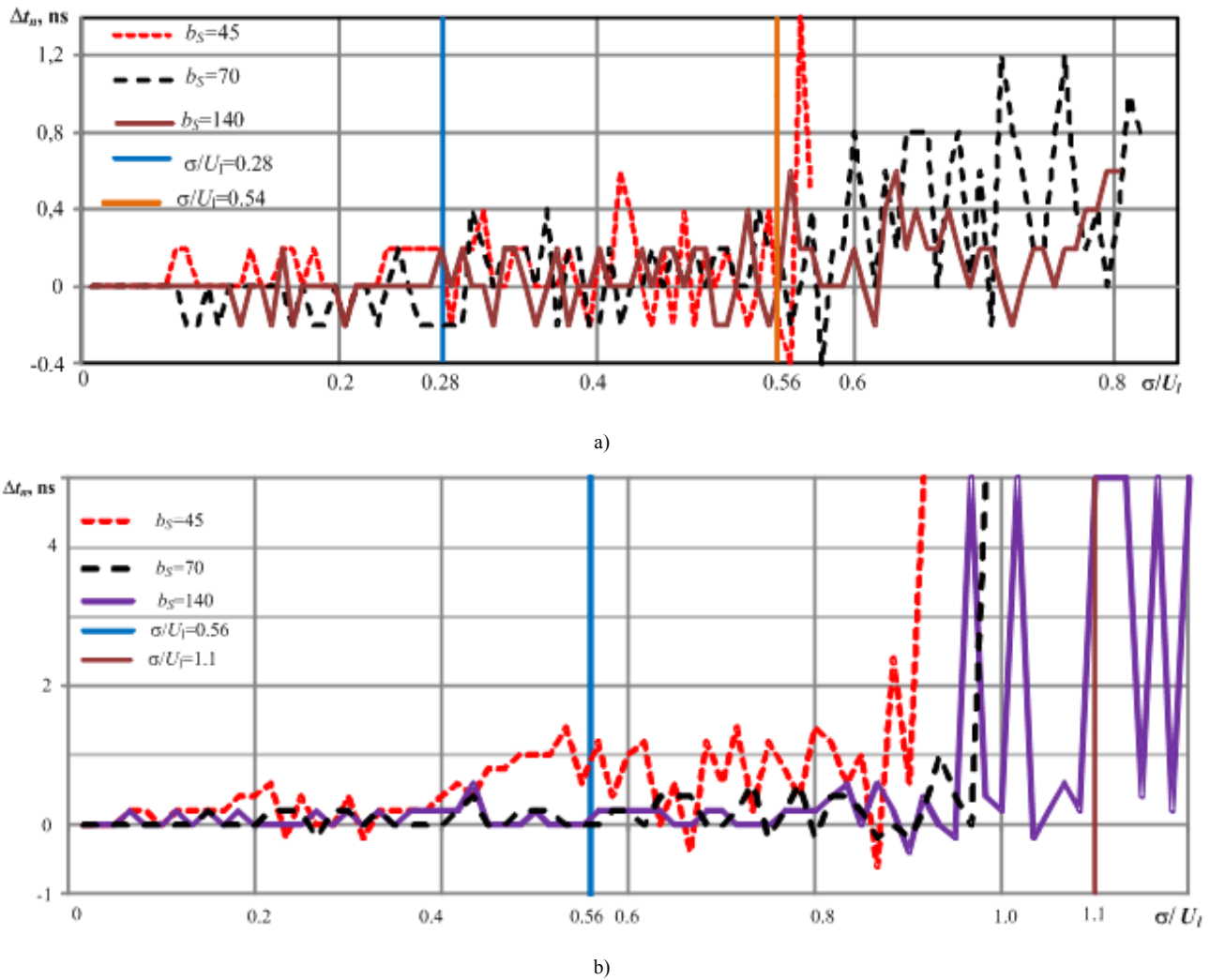


Figure 6. Dependence of an absolute error of the settling time measurement to the ratio of the noise level and 0.5 LSB readout levels; 100 signal realizations are used for filtering; signal ringing decrements are $b_S = 45; 70$ and 140 ; a) readout levels are $U_l = 61 \mu\text{V}$ (for 13 bit DAC); b) readout levels are $U_l = 30 \mu\text{V}$ (14 bit DAC)

4. Conclusions

1. Spectrum components of one realization of measurement signal (test signal of DAC) and internal noise of sampling converters, noise and disturbances of transmission lines and other sources of noise are overlapping. Therefore it is not possible to filter noise and remove errors generated by various sources of noise (internal noise, noise generated in signal transmission lines and so on) from settling time measurement result using standard filtering techniques. Combining n_r realizations of the test signal with random internal noise to the pseudo-periodic sequence and setting periodization parameters right it is possible to get a pseudo-periodic test signal where the test signal spectral components are separated enough from the random noise. This makes partial filtering of the test signal feasible.
2. A brick-wall digital comb filter in frequency domain has been developed and implemented for filtering of the noise generated in sampling converter, signal transmission lines and other sources of noise while keeping the test signal not distorted. The modeling of the process has shown that the filter developed is effectively reducing (about 10 times when using 75 to 100 realizations of the test signal for) low-frequency and white noise components.
3. DAC settling time measurement algorithm using digital brick-wall comb filter in frequency domain has been developed and implemented. The investigations of the algorithm presented that the errors of settling time measurement are not exceeding (+1.6 –0.6) ns if the ratio of the noise standard deviation magnitude and readout levels is up to 0.9.
4. The investigations has shown that highest errors of settling time measurement are obtained with low decrement of the ringing of the test signal ($b_s = 45$).

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