Universal Journal of Electrical and Electronic Engineering 3(3): 81-84, 2015 http://www.hrpub.org
DOI: 10.13189/ujeee.2015.030302

Fabrication Process of n-AlGaAs/GaAs Schottky Diodes for on-chip Direct Integrated with Dipole Antenna

Norfarariyanti Parimon*, Rosalyn R. Porle, Mazlina Mamat

Faculty of Engineering, University Malaysia Sabah, Malaysia

Abstract Schottky diodes are fabricated on n-Aluminium Gallium Arsenide / Gallium Arsenide (n-AlGaAs/GaAs) high-electron-mobility-transistor (HEMT) structure due to availability of high electron mobility and capability of fast switching performance. The processing steps used in the fabrication are the conventional steps used in standard GaAs processing. The ohmic and Schottky contacts of Schottky diodes are facilitated with ground-signal-ground (G-S-G) coplanar waveguide (CPW) transmission line structure so that it may provide the possibility of direct on-chip integration without insertion of a matching circuit with dipole antenna.

Keywords n-AlGaAs/GaAs, Schottky Diode, Dipole Antenna

1. Introduction

The Schottky diode is widely used in the electronics industry finding many uses as a general purpose rectifier. However it has come into its own function for radio frequency applications because of its high switching speed and high frequency capability. The most common element used in this Schottky diode design is silicon due to its well established fabrication processes and the second most abundant element in the Earth's crust.

Requirement for high speed, high frequency technologies, high mobility and high saturation velocity, GaAs is better compared to silicon. Heterojunctions that can typically be formed on GaAs substrates include AlGaAs/GaAs [1]. The n-AlGaAs/GaAs has been considered as the most promising material because of its stability and capability of making a good Schottky contact. This will be focused on the fabrication processes of Schottky diode to be used for direct integration with dipole antenna.

The energy band diagram and structure of n-AlGaAs/GaAs HEMT's [2] for fabrication process is shown in Figure 1. The two dimensional electron gas (2DEG) in n-AlGaAs/GaAs exhibits good transport properties and high electron velocities which is suitable for high-frequency devices [3].

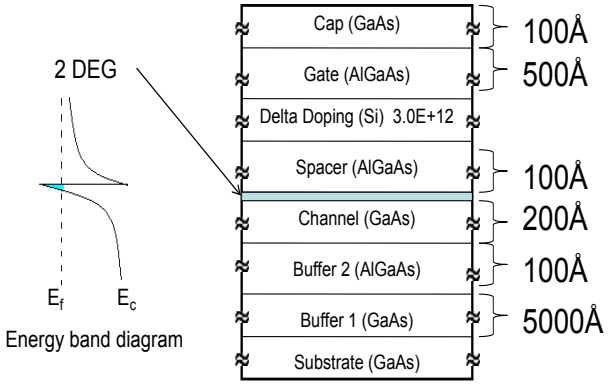

Figure 1. The energy band diagram and a cross section of n-AlGaAs/GaAs HEMT structure

Various kinds of integrated of Schottky diode and antenna have been developed using the impedance matching circuit [4]. Nowadays, this matching circuit can be avoided. Hence, in this fabrication process, the Schottky diode will fabricate without matching circuit for planar on-chip direct integration with dipole antenna.

Coplanar waveguide (CPW) is a term used to describe what really amounts to class of planar microwave transmission structure that comprises various arrays of conductors configured in the same geometric plane. The advantage of CPW is, it suitable as feeding line in fabrication of Schottky diode structure and dipole antenna. The transmission line is designed in a CPW for 150 µm pitch probes in order to suit the dimension of G-S-G Cascade Infinity-150 Microprober used in a measurement process.

CPW is formed from a conductor separated from a pair of ground planes, all on the same plane on a dielectric medium. CPW with finite dielectric thickness, h = 625 µm is used to be integrated with dipole antenna as transmission line [5].

The dependence of calculated characteristic impedance, Z_o as a function of gap, *a* and width, *b* is shown in Figure 2. The dimensions of *a* and *b* for the CPW are calculated based on the Wheeler's equation [6] have been chosen to be 60 µm and 90 µm, respectively, for the characteristic impedance, Z_o of 50 Ω [5].

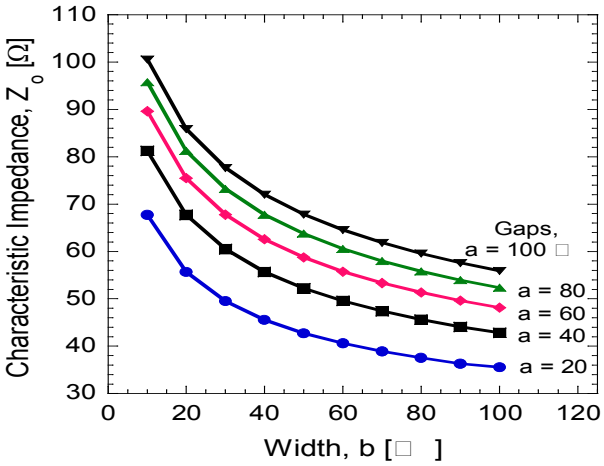

Figure 2. Characteristic impedance of CPW as a function of gap and width [5]

2. Fabrication Processes of Schottky Diode

The fabrication methods used here are based on the GaAs processing. Firstly, masks are used to create a specific pattern in a sequential manner. It can be made on glass or film substrates. In order to get a better result, glass mask is decided to use to form the pattern onto substrate.

The Schottky device fabrication layout is consists of 3 different glass mask layers designed. The first layer consists of alignment markers for processing subsequent layers and forming the mesa patterning. The second layer mask is designed for ohmic patterning, followed by third layer mask for Schottky patterning. To ensure that the masks are aligned properly in each layer of lithography, alignment markers are used as shown in Figure 3.

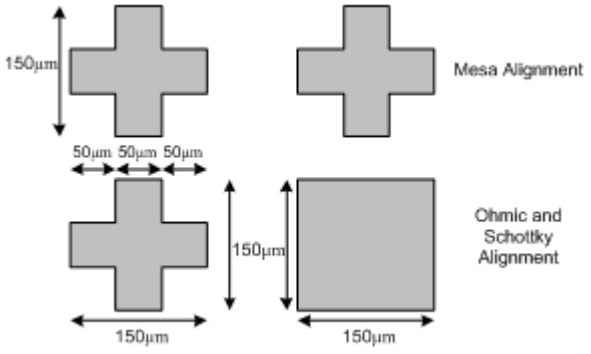

Figure 3. Alignment marker for mesa, ohmic and Schottky patterning

The processing steps are used in the Schottky diode fabrication is the conventional steps used in standard GaAs processing. These are pre-treatment, photolithography for mesa, ohmic and Schottky patterning, ultraviolet (UV) exposure and development process, wet etching methods for mesa formation, metal deposition for ohmic and Schottky contact on the wafer and lift-off technique [7]. The general flow of these processes is shown in Figure 4.

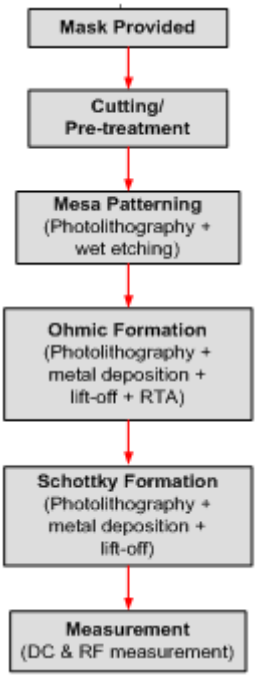

Figure 4. General flow of fabrication process

For pre-treatment, wafer is being cut using a diamond scriber or cutter for 1 cm x 1 cm. There are many design can be made on the wafer. It is essential that the wafer is thoroughly cleaned, degreased, and dried out. Cleaning the wafer chemically is to remove particulate matter like organic, ionic, and metallic impurities on the surface. It uses ethanol-acetone-ethanol in an ultrasonic bath for 5 minutes each, respectively, rinse with de-ionized (D.I) water and followed by dry with nitrogen blow.

2.1. Photolithography

Photolithography is the process of transferring geometric shapes on a mask to the surface of a semiconductor wafer or called resist covering. The steps that involved in the photolithography process are photoresist application including spinning resist over the wafer, soft baking, mask alignment, UV exposure and development, and hard baking. Photolithography is done to give a pattern each layer of the mask onto the wafer for mesa, ohmic, and Schottky patterning and finally, remaining resist is removed by developer. Once photolithography is completed, the patterned wafer is deposited with the selected metal by evaporation technique.

There are two type of photoresist, positive and negative, depending on how they are responding to radiation. As a general rule, positive resist has more advantages properties.

This resist offer higher resolution and allow more appropriate edge profiles for lift-off process. Hence, positive resist is normally the preferred choice for most aspects of GaAs processing and especially for this fabrication process [7]. Before the spinning started a dehydration bake at 100°C for 2 minutes in an oven need to be done. This further help the resist to be well stick onto the wafer surface by removing any residual moisture present. After the dehydration bake, the wafer must be cooled at room temperature for 1 to 5 minutes. The Primer adhesion is used to assist resist coating. Then, this wafer is coated with SPR 6810 resist by high speed centrifugal spinning. It is spinning typically at 500 rpm for 3 seconds and thereafter to 5000 rpm for 30 seconds.

Soft-baking plays a very critical role in photo-imaging. The photoresist coating becomes photo-sensitive only after soft-baking at 90 °C for 5 minutes. Then, it is cooled for 1 hour in room temperature before exposing. It is done to remove all the solvents that remained from the resist coating and improves adhesion. Before exposing, resist patterns are immersed in the developer for 15 seconds in order to harden the resist. The wafer must be rinsed to remove the developer using D.I water for 30 seconds, and then dried at room temperature for 1 hour.

One of the most important steps in the photolithography process is mask alignment. The mask is aligned with the wafer, so that the pattern can be transferred onto the wafer surface. With the alignment marks that are already on the substrate, the successive layers are matched and aligned.

The photoresist is exposed with high intensity UV light while the wafer is in contact position with the mask. After the wafer is exposed, the device is differentiated in the photoresist as regions of exposed and unexposed resist. The development process has to be in a proper time in order to get a good pattern. The pattern is developed by developer MFCD26 for 45 seconds and rinse with D.I water for 60 seconds. The wafer then is dried with nitrogen blow.

Hard-baking is the final step in the photolithography process. The wafer is hard-baked in the oven for 90°C for 5 minutes. This step is necessary in order to harden the photoresist and improve adhesion of the photoresist to the wafer surface, so that resist can endure etchant during mesa patterning. Then, resist is removed with a dip in MEK or remover 1165.

2.2. Wet Etching for Mesa Patterning

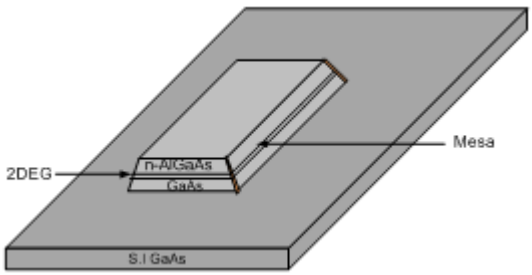

Figure 5. Mesa pattern

For mesa patterning, the wet etching step is included to form the pattern. The etchant prepared for etching process are sulfuric acid (H_2SO_4), hydrogen peroxide (H_2O_2), and D.I water. The ratio of H_2SO_4-H_2O_2-H_2O etchant composition is 8:1:1. After the mixing process, the temperature of etchant will increase rapidly up to 85～100°C. In order to decrease the temperature till reach to 25°C, the container is required to be covered with ice cubes around it. The etching time of the wafer is 18 seconds. The mesa pattern after etching process is shown in Figure 5.

2.3. Ohmic Patterning

Formation of the ohmic contacts has to be done before performing the Schottky contact formation because it requires a high temperature annealing process. The ohmic contact is deposited with Germanium/Aurum/Nickel/Aurum (Ge/Au/Ni/Au) using e-beam evaporator and lift-off process. The ohmic metallization need to be alloyed by rapid thermal annealing (RTA) process in N_2 ambient. The ohmic pattern is shown in Figure 6.

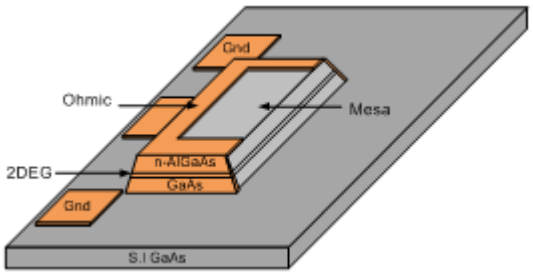

Figure 6. Ohmic pattern

2.4. Schottky Patterning

The Schottky contact is formed by Nickel/Aurum (Ni/Au) metallization. After the deposition of metals on the wafer, the lift-off process is applied, so that the unwanted metals are peeled off from the substrate. Figure 7 shows the illustration of the completed ohmic and Schottky pattern, while in Figure 8 shows top view of fabricated Schottky diode. It is fabricated on the n-AlGaAs/GaAs layered structure.

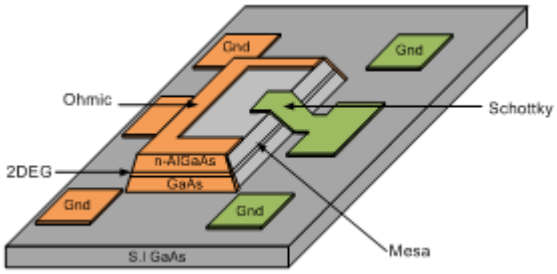

Figure 7. Ohmic and Schottky pattern [8]

Metal on the wafer will remain while metal on the resist will be removed. Lift-off can be accomplished by immersing

in methyl ethyl ketone (MEK).

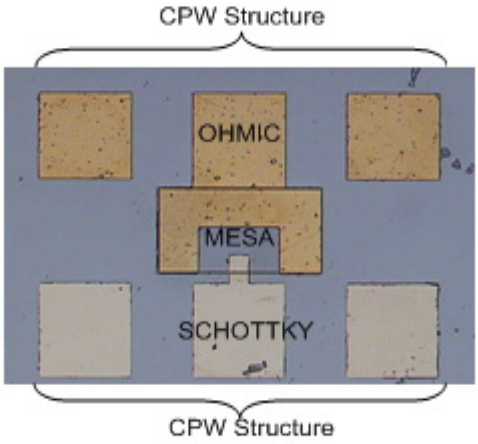

Figure 8. Fabricated Schottky Diode from top view [8]

3. Conclusions

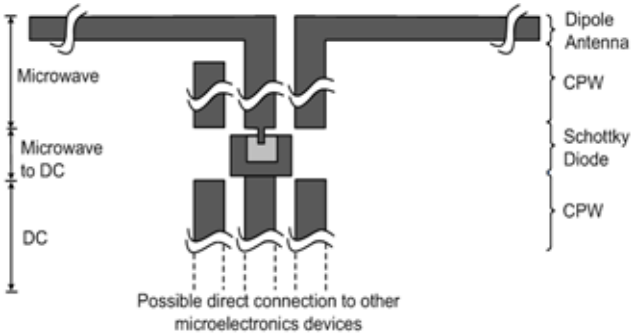

Figure 9. The illustrated of Schottky diode integrated with dipole antenna without impedance matching circuit [8]

A complete Schottky diode fabrication processes have been briefly explained. In this stage, an I-V characteristic of Schottky diode can be measured for further analysis. The possible direct connection between Schottky diode and dipole antenna designed on the same substrate is illustrated in Figure 9 [8]. Based on the design and obtained results of the dipole antenna [5] and Schottky diode, it is expected that direct integration via short CPW transmission line can be achieved without any impedance matching circuit. For this purpose, the behavior of the dipole antenna and Schottky diode has to be modeled at and around the operating frequency.

Acknowledgements

The authors would like to thank A. M. Hashim for his assistance and the Malaysia government and National Science Fellowship (NSF) for financial support.

REFERENCES

[1] M. Kuzuhara, S. Tanaka. GaAs-based high-frequency and high-speed devices, The Japan Society of Applied Physics, No. 7, 2003.

[2] Intelliepi.com. Intelligent Epitaxy Technology, Inc. 1250 E. Collins Blvd, Richardson, TX 75081, United States.

[3] T. W. Yoo, K. Chang. Theoretical and experimental development of 10 and 35 GHz rectennas, IEEE Transactions on Microwave Theory and Technique, Vol. 40, No. 6, pp. 1259-1266, 1992.

[4] J. Heikkinen, P. Salonen, M. Kivikoski. Planar rectennas for 2.4 GHz wireless power transfer, Proceeding of radio and wireless conference, Denver CO, pp. 63-66, 2000.

[5] F. Mustafa, A. M. Hashim, A. A Aziz, R. M Hashim. Planar dipole antenna analysis with various length, width and thickness for super high frequency range, 2009 IEEE Regional Symposium on Micro and Nano Electronic, 2009.

[6] R. Garg, P. Bhartia, I. Bahl, A. Ittiboon. Microstrip Antenna Design Handbook, Artech House Norwood, MA, 2001.

[7] G. B. Albert, I. H. A. Carol. Fabrication of GaAs Devices, The institution of Electrical Engineers, United Kingdom, 2005.

[8] F. Mustafa, A. M. Hashim, N. Parimon. RF Characteristics of Planar Dipole Antenna for Direct Integration with AlGaAs/GaAs Schottky Diode, International Symposium on Antenna and Propagation (ISAP), pp. 935-938, 2009.