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The Ringing and Overshoot of a Simulated Microstrip Transmission Line

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Abstract This paper presents the first of several Matlab codes to perform easy electromagnetic simulations by using those presented in [1]. All the codes have to be updated by using the newest version of the Matlab software, however, the only one presented shows the mighty and simplicity of all codes.

Keywords Signal Integrity, Transmission Lines, Distortion, Delay, Phase Shift-effects, Cross Talk, Ringing, Overshoot, Transients, False Switching, Timing, Signal Quality

1. Introduction

Planar transmission lines are at present time massively used in cell phones, tablets, laptop computers and other modern devices. To maintain the signal integrity and signal quality on those devices, the integrated circuits have to be massively integrated on little spaces generating problems as the Phase Shift-Effects, Cross Talk, Ringing, Overshoot, Transients, False Switching and others.

2. Background

Functionality increase has been and will continue to be the major driving force for the semiconductor industry. As a matter of fact, the spectacular success of IC industry in the past 30 years depends on the ability to continuously shrink the feature size of IC fabrication process and at the same time pack more devices on a single silicon die. However, when the main-stream fabrication technology is now moving to the 90-nm node, the feasibility of the monolithic integration paradigm is severely stumbled by the following factors.

Interconnection "Crisis": Historically, functionality to be integrated in a single chip at every technology generation always exceeds the capacity provided by pure scaling. To accommodate the extra transistors, chip size has always been increasing since the invention of the first integrated circuit [1]. The problem is that, interconnection length, especially worst-case interconnection length, has to increase as long as IC chip size is expanding. Starting from the 0.25 m generation, the interconnection delay of long on-chip wires has become the dominant part determining system performance [2]–[4]. As a result, the timing of global signals has become a critical concern. Unfortunately, interconnection delay is very hard to predict before the circuit is actually laid out. As a result, current synthesis-based VLSI design methodology often has difficulty to achieve timing closure.

Fabrication Cost: The extreme complexity of today's semiconductor process leads to a skyrocketing of the fabrication facility cost [5]. It has been reported that the cost of a single mask set and corresponding probe will soon reach $1 million [6], [7]. Meanwhile, modern system-on-chips (SoCs), especially those for wireless applications, typically integrates heterogeneous components. These components are originally targeted for different fabrication technologies. This further complicates the merged process and raises fabrication cost. For example, in a RF-CMOS process, the price of a finished wafer is higher than that of pure CMOS by at least 15% [8]. Meanwhile, for RF circuits, it is difficult to achieve further performance improvement and cost reduction by using a scaled technology. For instance, many analog transistors and passive components have to occupy a relatively constant die area to meet performance requirements no matter in which technology generation they are fabricated [8].

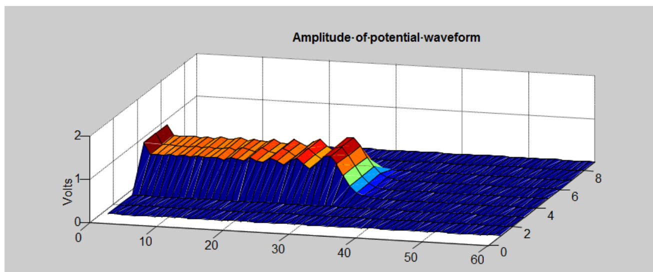
Memory Gap: Memory bandwidth has already become the limiting factor impeding the performance of general-purpose microprocessors and multimedia appliances, as well as other data-intensive applications. It has been reported that the processor performance has been improving by 35% annually from 1980 to 1986 and by 55% annually thereafter [9], [10]. In the same period, the access latency of DRAM has been improving by only 7% per year [9]. Now this problem is mainly addressed by introducing cache hierarchy and integrating memories with the logic on the same chip. For most current processors, at least 50% of the die area is occupied by cache memories [11]. Also, a

PDA-type phone could use as much as 128-Mb flash and 128-Mb DRAM [12].

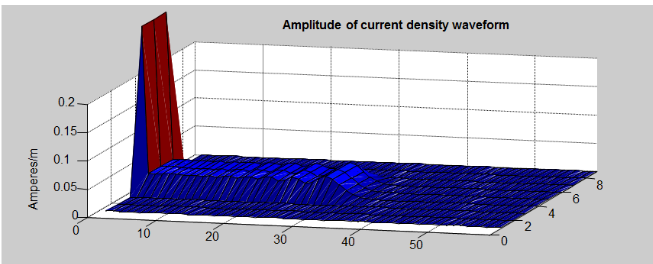
It must be indicated that the above problems are inherent to the monolithic integration. Therefore, the key question must be raised: How to build modern systems that avoid the shortcomings of monolithic SoC, while maintaining momentum in the increase of the functionality?

3. Conclusions

As can be seen by running the routine of [1] (page 61 of that reference), the behavior of a simulated microstrip transmission line after 100 time steps is clearly shown in Fig. 1.



Timesteps=100
Time(s)=1.4796e-10



Number of clls

Figure 1. Behavior of a simulated microstrip transmission line after 100 time steps.

```
% THE RINGING AND OVERSHOOT OF A SIMULATED MICROSTRIP TRANSMISSION LINE %

warning off


%% ACQUIRING DATA.
CO2=0;
%Note1: CO is the value for the connector in cm.

IV=9;
JV=59+CO2;
KV=3+3;
LV=59+CO2;
freqmi=0*1e9;
freqma=3*1e9;
freqce=(freqma+freqmi)/2;
freqstep=0.01*1e9;

%Permitividad de la microcinta.
epsrm=10.5;

%Permeabilidad en el vacio.
muz=4*pi*1e-7;

%Permitividad en el vacio.
epsz=8.854e-12;

cz=1/(sqrt(muz*epsz));

%Espesor del dieléctrico.
W1=0.001882;

%Valor en x de la micro cinta.
ddx=W1/3;

%Valor en y de la micro cinta.
ddy=ddx;

dt=ddx/(sqrt(2)*cz);

nsteps=input('Enter the number of timesteps: ');
sel= questdlg('¿Graficar en 2D o 3D?', 'INFO', '2-D', '3-D', '3-D');

nfreqs=((freqma-freqmi)/freqstep)+1;
freq(1:nfreqs)=freqmi:freqstep:freqma;
freqi(1:nfreqs)=freqma:-freqstep:freqmi;

arg(1:nfreqs)=2*pi*freq(1:nfreqs)*dt;
args(1:nfreqs)=2*pi*freq(1:nfreqs);

H=0.000635;
W1=0.001882;
Wf1=0.001882*1e3;
[ls1, cs1, Zo1, vpm] = minocodi(epsrm, epsz, H, W1);

Lvp1=((dt*vpm)*ls1)/(2*ddx);
Lp1=(ls1/2)+Lvp1;

Zo=Zo1;                       %Impedancia caracteristica.
Zs=Zo/3;%Zo;%3*Zo;%Zo/4;      %Impedancia de fuente.
Zl=0.0;%6.5*Zo;%Zo;%Zo+i*Zo;  %Impedancia de carga.
clc

v(1:IV,1:JV+1)=0;
jx(1:IV+1,1:JV)=0;
jy(1:IV,1:JV)=0;
t0=20;
spread=4;
T=0;
ini=1;
sal=1;
```

```
%% CYCLE FOR
for t=1:nsteps

        T=T+1;
        pulse=1;
        v(4:KV,1)=pulse;

jy(4:KV,2)=jy(4:KV,2)-((v(4:KV,3)-v(4:KV,2))*Lp1);
        v(4:KV,2)=v(4:KV,1)-(jy(4:KV,2)*mean(Zs));

jx(5:KV,1:LV)=jx(5:KV,1:LV)+(dt/(ls1*ddx))*(v(4:KV-1,
1:LV)-v(5:KV,1:LV));

jy(4:KV,1:LV)=jy(4:KV,1:LV)+(dt/(ls1*ddy))*(v(4:KV,1:
LV)-v(4:KV,2:LV+1));

v(4:KV,3:LV)=v(4:KV,3:LV)+(dt/(cs1*ddx))*(jx(4:KV,3:L
V)-jx(5:KV+1,3:LV)-jy(4:KV,3:LV)+jy(4:KV,2:LV-1));

jy(4:KV,LV)=jy(4:KV,LV)+((v(4:KV,LV)-v(4:KV,LV+1))
*Lp1);
        v(4:KV,LV+1)=jy(4:KV,LV)*mean(Zl);

        if   t==ini
           timestep=int2str(t);
           time=num2str(t*dt);

           if strcmp(sel,'2-D')
              %GRAFICA I
              subplot(2,1,1)
              surf(1:JV+1,1:IV,v);
              title('Amplitude of potential
waveform','FontWeight','Bold')
              zlabel('Volts')
              text(-10,0,-0.2,['Timesteps
=',timestep],'FontWeight','Bold')
              text(-10,0,-0.3,['Time(s)                    =
',time],'FontWeight','Bold')
              view([0,0])

              %GRÁFICA II
              subplot(2,1,2)
              surf(1:JV,1:IV,jy);
              title('Amplitude of current density
waveform','FontWeight','Bold')
              xlabel('Number of cells')
              zlabel('Amperes/m')
              view([0,0])
           end

           if strcmp(sel,'3-D')
             %GRÁFICA I
              subplot(2,1,1)
              surf(1:JV+1,1:IV,v);
              title('Amplitude of potential
waveform','FontWeight','Bold')
              zlabel('Volts')
              %INFORMACIÓN DE TIMESTEPS Y
TIEMPO
              text(-((JV+1)/(5)),0,-1.5,['Timesteps
=',timestep],'FontWeight','Bold')
             text(-((JV+1)/(5)),0,-2.0,['Time(s) =
',time],'FontWeight','Bold')
              axis([0 JV+1 0 IV 0.0 2.0])
              view([15,45])
              %colorbar('east');

              %GRÁFICA II
              subplot(2,1,2)
              surf(1:JV,1:IV,jy);
              title('Amplitude of current density
waveform','FontWeight','Bold')
              xlabel('Number of cells')
              zlabel('Amperes/m')
              %ACTIVAR PARA VISTA EN 2-D
              %view([0,0])
              %ACTIVAR PARA VISTAN EN 3-D
              axis([0 JV 0 IV 0.0 0.2])
              view([15,30])
              %colorbar('east');
           end
           pause(0.01)
           ini=ini+sal;

        else
        end
  end
```

REFERENCES

[1] A. Dueñas Jiménez, 2-D Electromagnetic Simulation of Passive Microstrip Circuits, Boca Raton, FL: CRC Press a Taylor and Francis Company, 2009, 274 pp.

[2] G. Breed, High Frequency Electronics, Copyright © 2010 Summit Technical Media, LLC, 58-60.

[3] M. E. Hines and H. E. Stinhelfer, Time domain Oscillographic Microwave Network Analysis Using Frequency-Domain Data, 276-281, IEEE Transactions on Microwave Theory and Techniques, vol. MTT-22, No. 3, March, 1974.

[4] ALTERA, Application Note 224, High-Speed Board Layout Guidellines, September 2003, ver. 1.1, 34 pp.

[5] D. Brooks, Adjusting Signal Timing (Part 1), Technical Publication, October 2003, Mentor Graphics, 9 pp.

[6] D. Brooks, Controlling Impedances When Nets Branch Out, Technical Publication, March, 2005, Mentor Graphics, 6 pp.

[7] Y. Deng and W. P. Maly, 2.5- Dimensional VLSI System Integration, IEEE Transactions on Very Large Scale

Integration (VLSI) Systems, vol. 13, No. 6, June, 2005.

[8] Intel EP80579 Integrated Processor Product Line Platform, Design Guide, 2008, 349 pp.

[9] Souri and K. C. Saraswat, Interconnect performance modeling for 3D integrated circuits with multiple Si layers, Interconnect Technology, 1999.IEEE International Conference, pp. 24-26, 1999.

[10] To be published in the Proceedings of the IEEE, May 2001, 57 pp.

[11] 3-D Ics: A Novel Chip Design for Improving Deep-Submicrometer Interconnect Performance and Systems – on-Chip Integration, Proceedings of the IEEE, vol. 89, No. 5, May 2001.

[12] Bridging the Gap Between the Digital and Real Worlds: the Expanding Role of Analog Interface Technologies, B. Murari, STMicroelectronics, Cornaredo, Italy, 2003 IEEE International Solid-State Circuits Conference, 19 pp.