

# A Novel Verilog-A model of Spin Torque Transfer Magnetic Tunnel Junction

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**Abstract** A novel simple and efficient model of Spin Torque Transfer Magnetic Tunnel Junction (STT-MTJ) using Verilog-A is presented. The model accurately emulates the main properties of an STT-MTJ which includes Tunnel Magneto Resistance Ratio (TMR), its dependence on the voltage bias and the critical switching current. The novelty of the model lies in the fact that the voltage dependence of TMR has been modeled using a single equation. The model can be used for faster simulations of hybrid Magnetic CMOS circuits and in various other wide range of applications. The model was developed in Verilog-A and verified using Synopsys Hspice 2010.

**Keywords** Behavioural modelling, Magnetic Tunnel Junction, MTJ, Spin Torque Transfer RAM, Verilog-A

## 1. Introduction

With the evolution of supercomputers to handle complex computing tasks there is a requirement of a universal memory [1], as traditional memory technologies like SRAM, DRAM & Flash cannot serve the same purpose due to various limitations like low density in SRAM, volatility of data in DRAM and low operation speed & less endurance of Flash [2]&[3]. To serve this purpose and to overcome the limitations in the traditional memory technologies nowadays Spin Torque Transfer Random Access Memory (STT-RAM) is gaining popularity as a future universal memory. STT-RAM promises to provide key features of a universal memory [4] like high density, low cost, high speed, low operation & storage power requirements, random accessibility, non-volatility and unlimited endurance, a memory technology which can handle all the computing requirements of a device.

The basic storage element (Fig. 1) [5] which is used for storage in a magnetic random access memory (MRAM) is a magnetic tunnel junction (MTJ). The basic structure of a MTJ consists of an insulating layer called “tunnel barrier” inserted between two ferromagnetic layers: the “free layer”

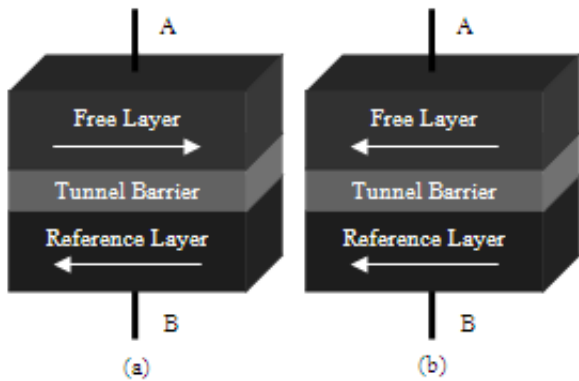
and the “reference layer”. The magnetization direction of the reference or the fixed layer remains unchanged and the data is stored by switching the magnetisation direction of the free layer. The MTJ is formed by an insulating tunnel barrier sandwiched between two ferromagnetic electrodes (the free layer and the fixed reference layer). The free layer electrode is usually made up of metals such as Fe, Co & Ni and their alloys. The fixed layer is antiferromagnetically coupled with the pinned layer through Ru layer to form a SAF (Synthetic Anti Ferro magnet), the pinned layer is further coupled with a antiferromagnetic pinning layer [6]. This type of structure makes the free layer easy to write while the fixed layer remains unchanged.

MTJ is the basic building block for the future universal memories. The computer simulations has a great role in the design of any such system and the accuracy of the simulation results depends on how accurate device models are used for the simulations. Previously Linda M *et al.* has given a Verilog-A model of a MRAM cell [7] using the Field driven MTJ. Zhao *et al.* created a Verilog-A model of STT-MTJ [8], but the parameters used were related to each other using complex equations and the code was not disclosed in the paper. A circuit base model of STT-MTJ was given by Harms *et al.* [9], but the characteristics of their model can not perfectly match the experimental data. Lee *et al.* [10] has also given a circuit base model of the STT-MTJ. In this paper a simple and accurate behavioral model of STT-MTJ is presented using Verilog-A. This model uses a single equation (Eq. 3.1) to show the voltage bias dependence of TMR dividing it into three operating regions that are Parallel region, Antiparallel region with Positive bias and Antiparallel region with negative bias. This model can be used for efficient simulations of Hybrid Magnetic CMOS circuits in a faster way.

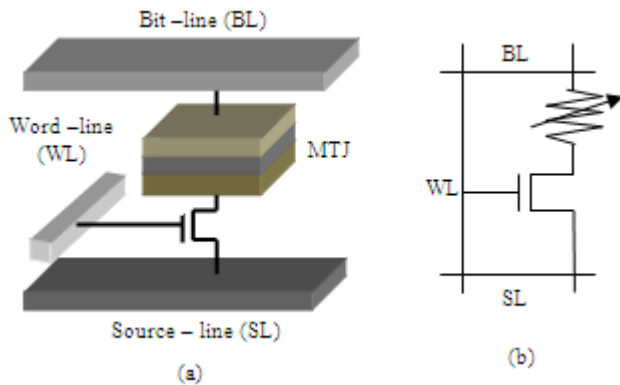
## 2. Spin Torque Transfer Magnetic Tunnel Junction (STT-MTJ)

The MTJ offers a low resistance when the two layers (free layer and reference layer) are magnetized in the same

direction, called the “parallel state” and it offers a high resistance when the direction of magnetization of both the layers is opposite, called the “antiparallel state”, Fig. 1 shows the two states of a MTJ. MRAM bit cell is formed by adding a read transistor (NMOS transistor) in series with the MTJ (Fig.2), the connections to the bit cells are named as bit-line (BL), source-line (SL) and word-line (WL). The data is read as ‘1’ if the MTJ offers a low resistance and a ‘0’ if the MTJ offers a high resistance or vice versa for negative logic.



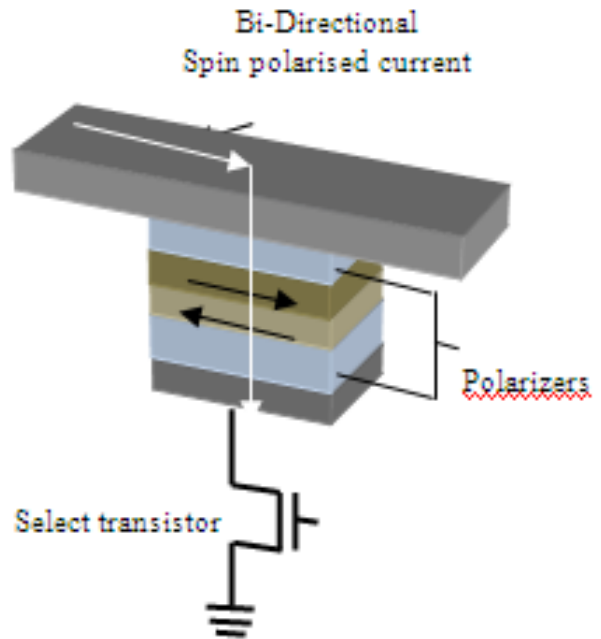
**Figure 1.** MTJ states (a) Antiparallel (high resistance) (b) Parallel (Low Resistance).



**Figure 2.** (a) MRAM bit cell (b) Equivalent schematic.

In the first generation of MTJ’s the data is written (free layer is toggled) using externally applied magnetic field which is produced using two on chip metal lines. This technique is known as Field Induced Magnetic Switching (FIMS). The data is written on to bit cell by driving a strong electric current through both the metal lines, producing a threshold field at the cross point of the lines. All the other neighboring bit cells are exposed to little more than half the threshold field, which can cause an unwanted overwrite in the neighboring bit cells. This phenomenon is known as the “half select” problem, the most encountered in FIMS technique. To take care of the “half select” problem, the bit cell must be at a proper distance and the threshold must be high so that any external disturbance is unable to change the bit cell. In 1998 it was experimentally shown that high density of spin polarized current can force the ferromagnetic layer to align in a particular direction [10]. STT switching mechanism uses both the preservation of spin direction

during electron transit across the spacer and the conservation of angular momentum. The current is spin polarized by adding a polarizing layer as shown in Fig. 3 or by the reference layer itself. The STT-MTJ has a critical switching current ( $I_c$ ), when  $I_c$  is applied on MTJ for a particular time period the current density in a MTJ reaches the critical current density ( $J_c$ ) and the MTJ switches it’s state. The switching to parallel or anti-parallel state depends upon the direction of current applied. While reading the data from MTJ, current lower than  $I_c$  is applied.



**Figure 3.** Spin torque transfer MTJ

The STT MTJ has two advantages over other writing schemes; the first advantage is that STT switching eliminates the need for additional write lines, thereby simplifying the circuitry used to control the device. The second advantage is that STT switching is dependent on the current density [9]. A STT-MTJ is shown in Fig. 3.

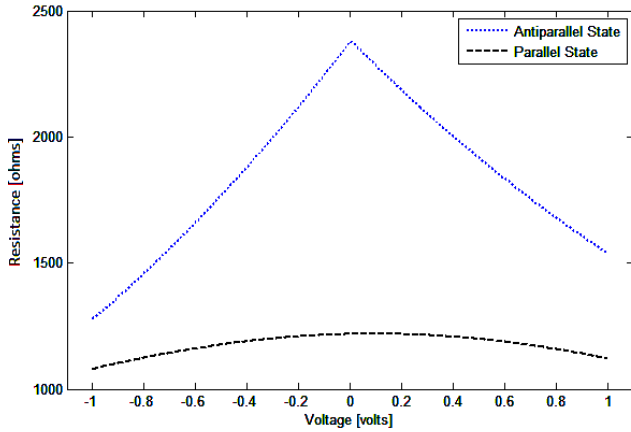
### 3. Properties of STT MTJ

#### 3.1. TMR (Tunnel Magneto Resistance Ratio) and Its Bias Dependence

The MTJs exhibits a high difference in parallel and antiparallel resistances represented as  $R_p$  &  $R_{AP}$  respectively. This difference is due to the coherent tunneling [11]. The ratio between the two resistance values is named Tunnel Magneto Resistance Ratio (TMR) and defined in Eq. (3.1). Recent research into spin-dependent tunneling in transition-metal-based MTJs has resulted in TMRs that have surpassed 500% at room temperature [12].

$$TMR = \frac{R_{AP} - R_P}{R_P} \quad (3.1)$$

One of the properties of a MTJ is that this ratio changes with the bias voltage ( $v$ ) on the MTJ. Increasing the bias causes a sharp decrease in  $R_p$  which is also asymmetric for the positive and negative bias voltages; in antiparallel state the resistance  $R_{AP}$  remains almost unchanged with the bias voltage. Fig. 4 shows the change in resistances with respect to bias voltages. Many mechanisms were proposed to mathematically prove this dependence but no model was able to reveal all the parameters which can give the relation between the TMR and the voltage bias.

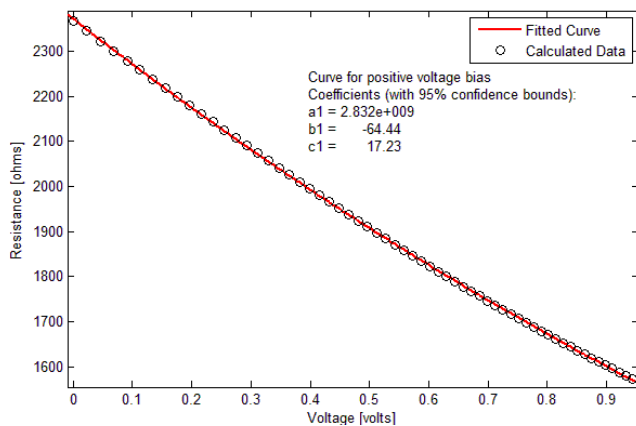


**Figure 4.** Voltage bias dependence of resistance in antiparallel state (upper curve), voltage bias dependence of resistance in parallel state (lower curve).

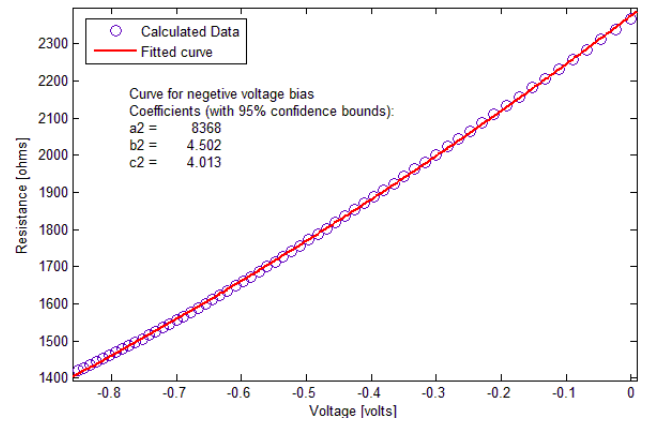
The available data from the previous models [9] & [10] are fitted using the Gaussian Function Eq. (3.2).

$$R = a \times e^{-\left(\frac{v-b}{c}\right)^2} \quad (3.2)$$

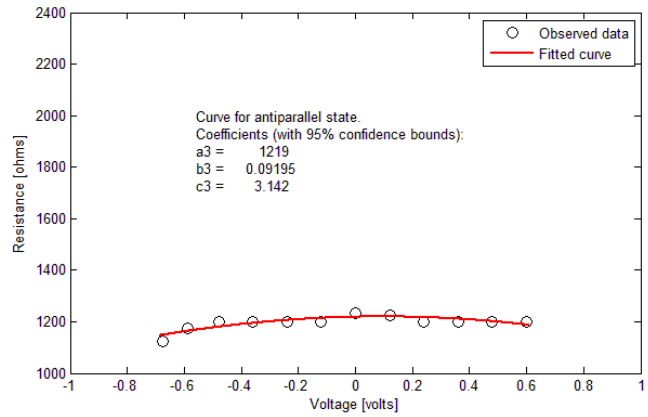
Where  $R$  is the resistance of MTJ and  $a$ ,  $b$  and  $c$  are the fitting parameters. The complete characteristics is fitted in this equation in three separate parts that are antiparallel state with positive voltage bias, antiparallel state with negative voltage bias and parallel state, as shown in Fig. 5, 6 & 7 respectively. The data from the previous models is shown as circles and the fitted curve as a line in these figures.



**Figure 5.** Available data from the previous model and fitted curve using Gaussian function in antiparallel state with positive voltage bias.



**Figure 6.** Available data from the previous model and fitted curve using Gaussian function in antiparallel state with negative voltage bias.



**Figure 7.** Available data from the previous model and fitted curve using Gaussian function in parallel state.

### 3.2. Critical switching current ( $I_C$ )

The critical switching current is the most important property of the MTJ as it represents in which state (parallel or antiparallel) the MTJ will remain. The critical switching current ( $I_C$ ) is defined as a function of switching time ( $\tau$ ) and operating temperature ( $T$ ), as shown in Eq.3.3 [13].

$$I_C = I_{C0} \left\{ 1 - \left( \frac{kT}{E} \right) \ln \left( \frac{\tau}{\tau_0} \right) \right\} \quad (3.3)$$

Where  $\tau_0$  is the inverse of write attempt frequency,  $k$  is the Boltzmann constant,  $E$  is barrier height and  $I_{C0}$  is critical current at zero Kelvin.

In this model the critical switching currents at room temperature are calculated taking the thermal stability coefficient  $E/kT$  equals to 22 with the write pulse width  $\tau$  equals to 10ns and the inverse of write attempt frequency  $\tau_0$  equals to 1ns. The values of switching current in parallel and antiparallel states were  $350\mu A$  and  $-450\mu A$  respectively and the corresponding values of switching voltages in parallel and antiparallel states were 0.585V and -0.675V respectively.

### 4. Verilog-A model

All of the properties of STT-MTJ explained in Sec.III has been modeled using Verilog-A. Verilog-A provides the best support for behavioral modeling of both electrical and non electrical systems. The model uses electrical discipline already defined in the language to access the nodal voltages and currents of the two terminal device. It takes in the applied voltage, perform calculations and assigns the calculated current using a current assignment statement. The complete Pseudo code used to model the device.is given below.

- Step 1- Read the value of input voltage from the input terminals.
- Step 2- Using the input voltage to determine in which region the MTJ is operating that is parallel state, antiparallel state with positive bias or antiparallel state with negative bias.
- Step 3- Calculate the value of resistance at the voltage using Equation 3.1 and values of fitting parameters(a, b and c) for that region.
- Step 4- Calculate the value of current using voltage and the resistance.
- Step 5- Assign the value of current to the nodes using a current assignment Statement.

- Step 6- Repeat the steps from Step 1.
- 5. Transient Simulation

The model was verified by running transient simulation in Synopsys Hspice simulator. The model was able to accurately show the characteristics of a STT-MTJ. The resistance varies with the voltage as predicted by the model, it also verifies the switching of MTJ from parallel to antiparallel and vice-versa. Observing the simulation results one can clearly notice the parallel and antiparallel states of the model. The simulation output if shown in Fig. 8.

### 6. Conclusion

A novel and simple model of a Spin Torque Transfer Magnetic Tunnel Junction was presented in this paper. The model accurately emulated the main characteristics of a STT-MTJ such as its TMR and the voltage dependence of its Resistance. The model can be used for faster simulations of hybrid Magnetic CMOS circuits such as MRAMs, nonvolatile Flip-Flops and many other related devices. The model can easily be improved to show the other properties of MTJ such as temperature dependence of the TMR and dynamic switching based on some other parameters.

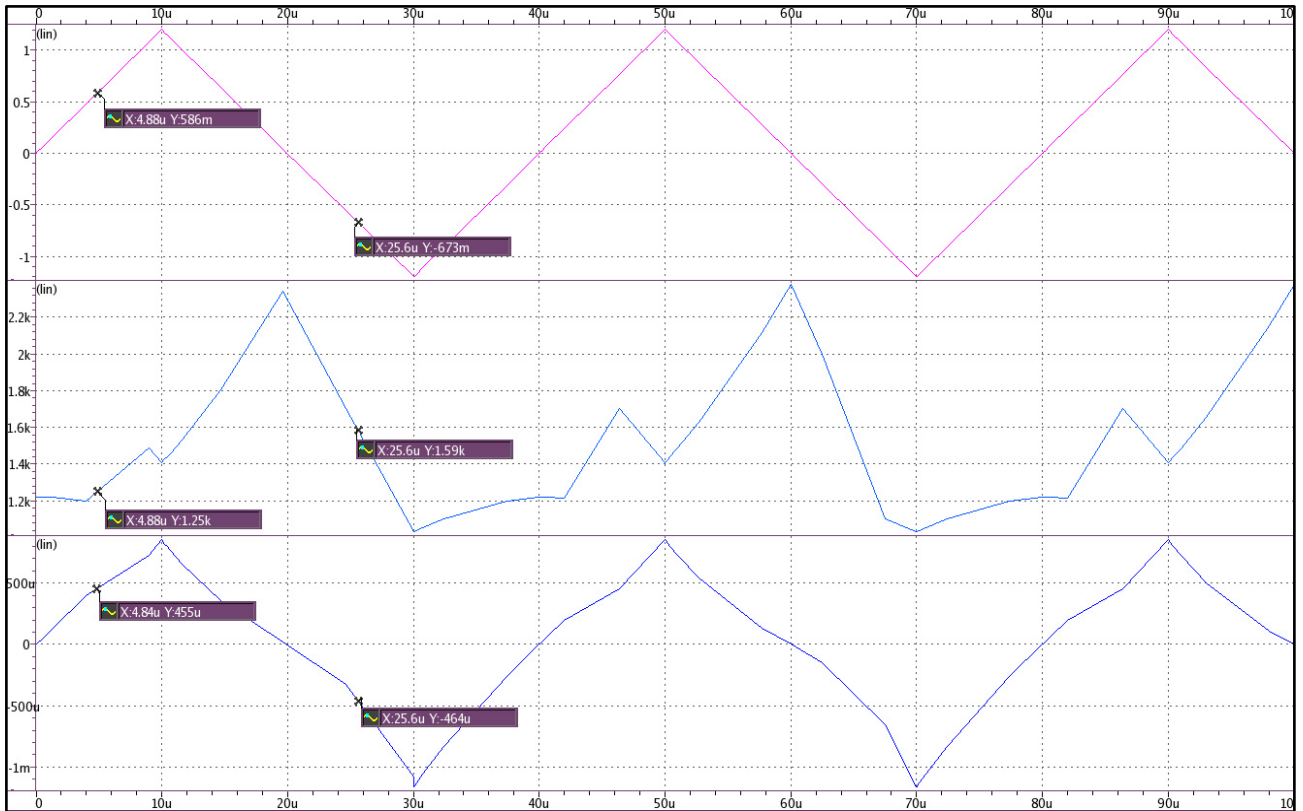


Figure. 8. Transient simulation results of the model applied Voltage(volts) top, model resistance middle & measured Current bottom.

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