Universal Journal of Electrical and Electronic Engineering 1(2): 11-15, 2013 http://www.hrpub.org
DOI: 10.13189/ujeee.2013.010201

Application of Distribution Static Compensator (D-STATCOM) to Voltage Sag Mitigation

H. Molavi[1,*], M. M. Ardehali[2]

[1]Institute of technology, Sharif University, Tehran, Iran
[2]Electrical Department, Amirkabir University, Tehran, Iran
*Corresponding Author: hmolavi@aut.ac.ir

Abstract This paper presents a study of a D-STATCOM (Distribution Static Compensator) used for mitigating voltage sag. The basic idea of the voltage sag mitigation, using a D-STATCOM is to dynamically inject a current of desired amplitude, frequency and phase into the grid line. The proposed method extracts the active and reactive parts of the positive- and negative-sequence component for generating reference values of current that need to be injected into the point of connection D-STATCOM in order to compensate the voltage errors. The proposed method offers structural simplicity and less calculation complexity. Simulation results indicate that this method is effective and D-STATCOM has good performance to mitigate the voltage sag.

Keywords Voltage Sag, D-STATCOM, D-Q Controller

1. Introduction

Voltage sag is a reduction between 10 and 90%in rms voltage with a duration between 0.5 cycles and 1 min (although voltage sag depth and duration typically range from 80 to 90% and 0.5 to 30 cycles, respectively) [1]. Voltage sags are the most important power quality (PQ) problems that many industries and utilities face it. Among different types of disturbances occurring in power system, voltage sag is known to produce the most devastating impact on the loads [2]. Studies show that 92% of all disturbances in the electrical power distribution systems are voltage sags, transients, and momentary interruptions [3, 4]. Voltage sags are not tolerated by sensitive equipment used in modern industrial plants such as process controllers; programmable logic controllers (PLC), adjustable speed drive (ASD) and robotics [5]. Various methods have been applied to reduce or mitigate voltage sags. The conventional methods are by using capacitor banks, introduction of new parallel feeders and by installing uninterruptible power supplies (UPS). Recently D-STATCOM has emerged as a promising device to provide not only for voltage sag mitigation but also for a host of other power quality solutions such as voltage stabilization, flicker suppression, power factor correction, and harmonic control [6]. D-STATCOM is a shunt connected device that generates a balanced set of three sinusoidal voltage or current at the fundamental frequency [7]. DSTATCOM configuration consists of a VSC that converts voltage across the storage device into a set of three-phase ac output voltages. These voltages are in phase and coupled with the ac system of network through the reactance of the coupling transformer [8]. In [9], a repetitive-based controller for a D- STATCOM is presented that compensate reactive power, but it offers more calculation complexity. [10], presented a D-STATCOM control algorithm which enables seperate positive and negative sequence currents, but the presented method needs more time than the control method that perenetd in this paper.

This paper presents a study of a D-STATCOM (Distribution Static Compensator) used for mitigating voltage sag. The control object of D-STATCOM is that the line voltages at the normal operation only include positive sequence. The control method is made up of DC voltage controller and current controller.

The rest of the paper is organized as follows: section II present the D-STATCOM description. Section III explains the control method. The obtain simulation results are discussed in section IV and finally, section V concludes the paper.

2. Description of the D-STATCOM

Figure.1 shows the schematic representation of D-STATCOM. The basic electronic block of the D-STATCOM is the voltage source inverter that converts an input dc voltage into a three-phase output voltage at fundamental frequency and the dc link voltage is provided by capacitor.

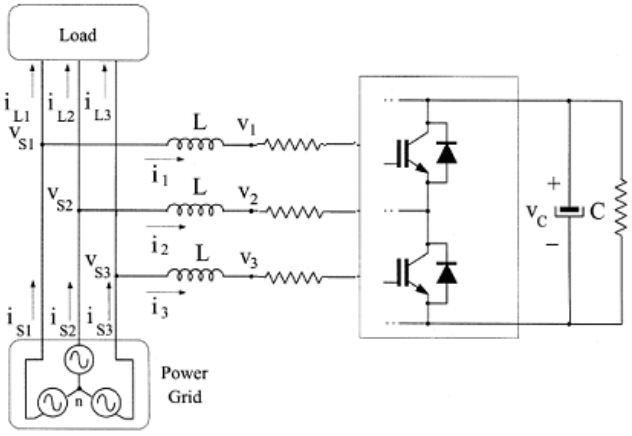

Figure 1. schematic representation of D-STATCOM

In the unbalanced conditions the line voltage is equal to the sum of negative and positive sequence so we will have:

$$V_{s1} = \sqrt{2}V_{sp}\cos(\omega t) + \sqrt{2}V_{sn}\cos(\omega t + \varphi_n) \quad (1)$$

$$V_{s2} = \sqrt{2}V_{sp}\cos(\omega t - \frac{2\pi}{3}) + \sqrt{2}V_{sn}\cos(\omega t + \frac{2\pi}{3} + \varphi_n) \quad (2)$$

$$V_{s1} = \sqrt{2}V_{sp}\cos(\omega t + \frac{2\pi}{3}) + \sqrt{2}V_{sn}\cos(\omega t - \frac{2\pi}{3} + \varphi_n) \quad (3)$$

In the above equation V_{sp} and V_{Sn} are the RMS of positive and negative sequence component of the line voltages, respectively. By applying Kirchoff's Voltage Law (KVL) we will have:

$$L\frac{di_1}{dt} + R_f i_1 = V_{s1} - V_1 \quad (4)$$

$$L\frac{di_2}{dt} + R_f i_2 = V_{s2} - V_2 \quad (5)$$

$$L\frac{di_3}{dt} + R_f i_3 = V_{s3} - V_3 \quad (6)$$

Applying Kirchoff's Current Law (KCL) satisfy the fallow equations:

$$i_{s1} = i_{L1} + i_1 \quad (7)$$

$$i_{s2} = i_{L2} + i_2 \quad (8)$$

$$i_{s3} = i_{L3} + i_3 \quad (9)$$

By combining the Eqs (4-6) with Eqs (7-9) we will have:

$$L\frac{di_{s1}}{dt} = L\frac{di_{L1}}{dt} + V_{s1} - V_1 - R_f i_{s1} + R_f i_{L1} \quad (10)$$

$$L\frac{di_{s2}}{dt} = L\frac{di_{L2}}{dt} + V_{s2} - V_2 - R_f i_{s2} + R_f i_{L2} \quad (11)$$

$$L\frac{di_{s3}}{dt} = L\frac{di_{L3}}{dt} + V_{s3} - V_3 - R_f i_{s3} + R_f i_{L3} \quad (12)$$

The model transformed from 'abc' frame into 'dq' frame is given by:

$$L\frac{d}{dt}\begin{bmatrix} i_{sd} \\ i_{sq} \end{bmatrix} = -\omega L\begin{bmatrix} -i_{sq} \\ i_{sd} \end{bmatrix} + \begin{bmatrix} V_{sd} \\ V_{sq} \end{bmatrix} - \begin{bmatrix} V_{ld} \\ V_{lq} \end{bmatrix} + \omega L\begin{bmatrix} -i_{Lq} \\ i_{Ld} \end{bmatrix} + L\frac{d}{dt}\begin{bmatrix} i_{Ld} \\ i_{Lq} \end{bmatrix} - R_f\begin{bmatrix} i_{sd} \\ i_{sq} \end{bmatrix} + R_f\begin{bmatrix} i_{ld} \\ i_{lq} \end{bmatrix} \quad (13)$$

In (13) the parasite resistance R_f is very small so that we have:

$$\boldsymbol{R}_f \begin{bmatrix} \boldsymbol{i}_{ld} \\ \boldsymbol{i}_{lq} \end{bmatrix} = \mathbf{O} \quad (14)$$

The switch frequency is much higher than line frequency, so the changes of $\boldsymbol{i}_{ld}$ and $\boldsymbol{i}_{lq}$ in a switch period can be omitted. Thus, we have:

$$\boldsymbol{L}\frac{\boldsymbol{d}}{\boldsymbol{dt}}\begin{bmatrix} \boldsymbol{i}_{ld} \\ \boldsymbol{i}_{lq} \end{bmatrix} = \mathbf{O} \quad (15)$$

According to (14) and (15) we have:

$$L\frac{d}{dt}\begin{bmatrix} i_{sd} \\ i_{sq} \end{bmatrix} + R_f\begin{bmatrix} i_{sd} \\ i_{sq} \end{bmatrix} = \begin{bmatrix} V_{sd} \\ V_{sq} \end{bmatrix} - \omega L\begin{bmatrix} -i_{sq} + i_{Lq} \\ i_{sd} - i_{ld} \end{bmatrix} - \begin{bmatrix} V_d \\ V_q \end{bmatrix} \quad (16)$$

3. Control Method

3.1. Extraction the Positive Component

In order to extraction the positive component; first consider the line voltage by a $\pi/3$ delay, as the below:

$$V_{s1-1} = \sqrt{2}V_{sp}\cos(\omega t - \pi/3) + \sqrt{2}V_{sn}\cos(\omega t + \varphi_n - \pi/3) \quad (17)$$

$$V_{s2-2} = \sqrt{2}V_{sp}\cos(\omega t - \pi) + \sqrt{2}V_{sn}\cos(\omega t + \varphi_n + \pi/3) \quad (18)$$

$$V_{s3-3} = \sqrt{2}V_{sp}\cos(\omega t + \pi/3) + \sqrt{2}V_{sn}\cos(\omega t + \varphi_n - \pi) \quad (19)$$

The negative component of V_{s1-s2} and V_{s2-s3} are equal to:

$$V_{s1-s2}^{-} = -(V_{s1} + V_{s3-3}) \quad (20)$$

$$V_{s2-s3}^{-} = -(V_{s3} + V_{s1-1}) \tag{21}$$

Eq (22) shows the relationship between line to line negative voltage and line to neutral negative voltages

$$\begin{bmatrix} V_{s1}^{-} \\ V_{s2}^{-} \\ V_{s3}^{-} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & 1 \\ -1 & 1 \\ -1 & -2 \end{bmatrix}\begin{bmatrix} V_{s1-s2}^{-} \\ V_{s2-s3}^{-} \end{bmatrix} \tag{22}$$

The line voltages are equal to sum of negative and positive sequence, so that :

$$V_s^{+} = V_s - V_s^{-} \tag{23}$$

Finally we can calculate the positive component by Eq (23).

3.2. Application of 'dq' Controllers

The proposed D-STATCOM controller consists of current and dc voltage controller. The dc voltage controller regulates the dc voltage at the required level and the current controller forces the D-STATCOM current to follow the references.

The transformation matrix from 's1s2s3' into 'dq' frame can be defined as follows [11]:

$$T = \frac{2}{3}\begin{bmatrix} \cos(\theta) & \cos(\theta+\frac{2}{3}\pi) & \cos(\theta-\frac{2}{3}\pi) \\ -\sin(\theta) & -\sin(\theta+\frac{2}{3}\pi) & -\sin(\theta-\frac{2}{3}\pi) \end{bmatrix} \tag{24}$$

We need the transformation of the Eqs (23) into conventional stationary $'\alpha\beta'$ coordinates and the transformation matrix is equal to [11]:

$$\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} = \sqrt{\frac{2}{3}}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} V_{s1}^{+} \\ V_{s2}^{+} \\ V_{s3}^{+} \end{bmatrix} \tag{25}$$

From the Eq (25) we will have:

$$\cos(\omega t) = \frac{x_\alpha}{\sqrt{x_\alpha^2 + x_\beta^2}} \tag{26}$$

$$\sin(\omega t) = \frac{x_\beta}{\sqrt{x_\alpha^2 + x_\beta^2}} \tag{27}$$

We need to decouple i_d and i_q for proper control design. Decoupling can be satisfied by introducing new parameters u_d and u_q.

$$u_d = V_{sd} - V_d + \omega L\, i_q \tag{28}$$

$$u_q = V_{sq} - V_q - \omega L\, i_d \tag{29}$$

Fig.2 shows the i_d and i_q controller; the transfer function of the closed loop of the controllers can be illustrated as below:

$$G_{cloop} = \frac{G_c G_r}{1 + G_c G_r} = \frac{K_P s + K_I}{S^2 + (\frac{R_f}{L_f} + K_P)s + K_I} \tag{30}$$

3.3. DC Voltage Controller

Regulation the DC voltage at desired value in the application of the D-STATCOM is very important. It is obvious that the regulation of DC voltage is carried out by charging and discharging of the capacitor. The relationship between V_{dc} and i_d can be written as the below:

$$\frac{d(V_{dc})^2}{dt} = -\frac{2(V_{dc})^2}{R_{dc}C} + \frac{3v_{d-PCC}\, i_d}{2CR_{dc}} \tag{31}$$

where, v_{d-PCC} is the d-axis component of point of common connection (PCC). By rearranging the Eq (30) we have:

$$\frac{d(V_{dc})^2}{dt} + \frac{2(V_{dc})^2}{R_{dc}C} = K \tag{32}$$

The schematic of the DC voltage controller is shown in Fig.3.

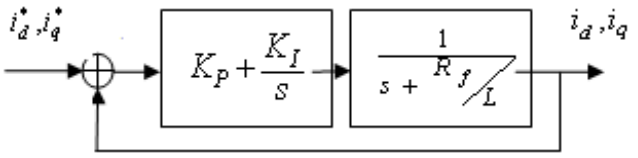

Figure 2. Equivalent block diagram of d-q controllers

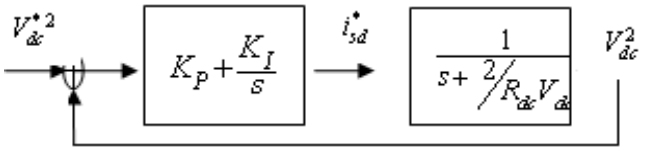

Figure 3. Block diagram of DC voltage controller

4. Reactive Power Controller

In the case of balanced three-phase voltage, the direct transformation of *abc* voltages into the *dq* reference frame will result in dc-quantities. Hence, the DSTATCOM can use a conventional PI-controller to control the injected reactive currents. However, if the grid voltage or the load voltages are unbalanced, a ripple of double the grid frequency will occur in the $d-q$ reference frame. In the case of unbalance three-phase voltages, breaking the voltage signals into positive- and negative- sequence components and then

transforming into *dq* synchronous reference frame results in dc-quantities and these *dq* feedback signals allow in control design reactive power control. Transformation of three-phase balance voltages with unity magnitude into the positive and negative *dq* synchronous reference frame results in dc-quantities with following values.

$$v_d^+ = 0\,pu\,, v_q^+ = 0\,pu$$

$$v_d^- = 0\,pu\,, v_q^- = 0\,pu$$

where v_d^+, v_q^+ are the positive sequence of voltage and v_d^-, v_q^- are the negative sequence of voltage. The controller's operation are based on above values, in other words the voltage sag in power network can be corrected by regulating positive and negative sequences to the above values.

5. Simulation Results

5.1. Test System

The simulation system is constructed according to Fig. 1 with the proposed compensation method. The circuit parameters are $V_s = 380\,V$, leakage reactance of each H-bridge $L = 10.1mH$, resistance of each H-bridge $R = 0.18ohm$ and $C = 440\mu F$, $f_s = 50Hz$. During the simulation, the unbalance load is operated with between phase A-C and between phases A-B.

5.2. Results and Discussions

Application of D-STATCOM to voltage sag mitigation is simulated in MATLAB/SIMULINK. Figure.4 shows the uncompensated voltage, from Fig.4 can be seen that the balanced sag (70%) occurs at 0.3 (sec). Fig.5 shows the compensated voltage which the voltage remains at 1 pu during the sag. Fig.6 shows the positive *dq* component and Fig.7 shows the negative *dq* component.

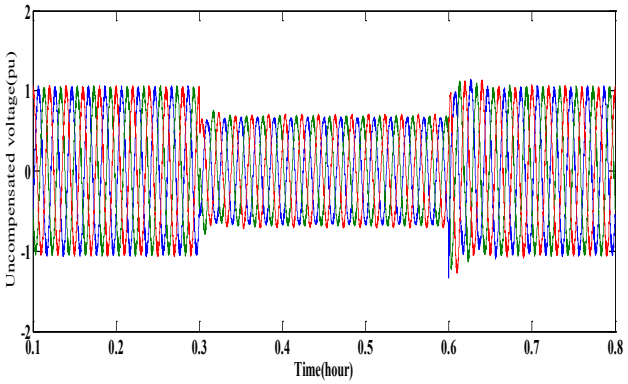

Figure 4. Uncompensated voltage

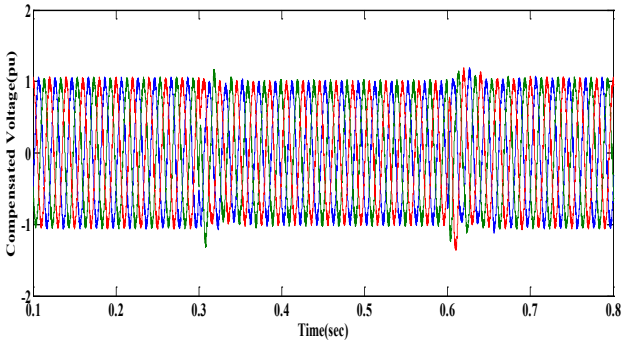

Figure 5. Compensated voltage

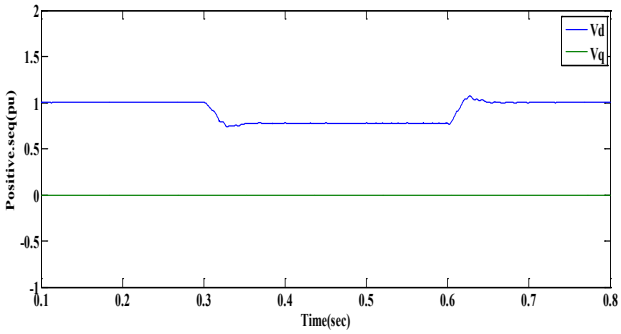

Figure 6. Positive *dq* component of voltage

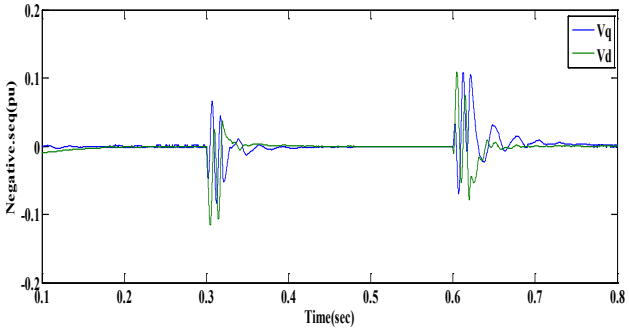

Figure 7. Negative *dq* component of voltage

6. Conclusion

This paper presented the operation of D-STATCOM to voltage sag mitigation. In order to mitigate voltage sag the positive and negative sequence is separated and the proposed method extracts the active and reactive parts of the positive- and negative-sequence component for generating reference values of current that need to be injected into the point of connection D-STATCOM in order to compensate the voltage errors. Simulation results show that D-STATCOM can be used for voltaje sag mitigation and has a good performance under voltaje sag.

REFERENCES

[1] R. C. Dugan, M. F. McGranaghan and H. W. Beaty,

*"*Electrical power systems quality*,"* McGraw Hill Companies, Inc., 1996.

[2] A. Ghosh, G. Ledwich, Power quality enhancement using custom power devices, Kluwer Academic Publishers, 2002, ISBN: 1402071809.

[3] T.A. Short, Electric Power Distribution Handbook, CRC Press, 2004.

[4] F. Shahnia, R. Majumder, A. Ghosh, G. Ledwich, F. Zare, "Voltage imbalance analysis in residential low voltage distribution networks with rooftop PVs" Elsevier, Electric Power Systems Research, Vol. 81, Issue 9, September 2011, pp 1805-1814.

[5] S. H. Hoseini, A, Nazarlu, E. Ebrahimi, "Application of D-STATCOM to Improve Distribution System Performance with Balanced and Unbalanced Fault Conditions" Electric Power and Energy Conference (EPEC), 2010 IEEE.

[6] Y.Liang and C.O.Nwankpa, "A new type of STATCOM based on cascading voltage-source inverters with phase-shifted unipolar SPWM," IEEE Trans. Industry Applications, Vol.35, No.5, Sept.Oct. 1999, pp.1118-1123.

[7] N.G. Hingorani and L. Gyugyi, "Understanding FACTS: Concepts and Technology of Flexible AC Transmission Systems", 1st edition, The Institute of Electrical and Electronics Engineers, 2000.

[8] D. Shen, W. Liu and Z. Wang, "Study on The Operation Performance of D-STATCOM Under Unbalanced and Distorted System Voltage," IEEE Power Engineering Society Winter Meeting., pp. 2630-2635.

[9] G. Escobar, A.A. Valdez, "A repetitive-based controller in stationary reference frame for D-Statcom in unbalanced operation", IEEE ISIE, July 2006.

[10] B. Blazic, I. Papic, "Improved D-StatCom Control for Operation With Unbalanced Currents and Voltages" IEEE TRANSACTIONS ON POWER DELIVERY, VOL. 21, NO. 1, January 2006.

[11] B.Blazic, I.Papic, "A new mathematical model and control of D-StatCom for operation under unbalanced conditions" Electric Power Systems Research, Volume 72, Issue 3, 15 December 2004, pp 279-287.