Effect of Nanowire-dielectric Interface on the Hysteresis of Solution Processed Silicon Nanowire FETs

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Abstract Silicon nanowires (Si NW) are ideal candidates for low-cost solution processed field effect transistors (FETs) due to the ability of nanowires to be dispersed in solvents, and demonstrated high charge carrier mobility. The interface between the nanowire and the dielectric plays a crucial role in the FET characteristics, and can be responsible for unwanted effects such as current hysteresis during device operation. Thus, optimal nanowire- dielectric interface is required for low-hysteresis FET performance. Here we show that NW FET hysteresis mostly depends on the nature of the dielectric material by directly comparing device characteristics of dual gate Si NW FETs with bottom SiO₂ gate dielectric and top hydrophobic fluoropolymer gate dielectric. As the transistor semiconducting nanowire channel is identical in both tops and bottom operational regimes, the performance differences originate from the nature of the nanowire-dielectric interface. Thus, very high 30 volt hysteresis is observed for forward and reverse gate bias scans with SiO₂ interface; however, hysteresis is significantly reduced to 6 volt for the fluoropolymer dielectric interface. The differences in hysteresis are ascribed to the polar OH⁻ groups present at SiO₂/Si nanowire interface, and mostly absent at fluoropolymer/Si nanowire interface. We further demonstrate that high density of charge traps for bottom gate SiO₂ interface ($1 \times 10^{13} \text{ cm}^{-2}$) is reduced by over an order of magnitude for top-fluoropolymer gate interface ($7.5 \times 10^{11} \text{ cm}^{-2}$), therefore highlighting the advantage of hydrophobic polymer gate dielectrics for nanowire field-effect transistor applications.

Keywords Nanowire Field-effect Transistor, Hysteresis, Silicon Nanowires, Nanowire Interface, Double Gate Transistor, Polymer Dielectric, Encapsulation

applications such as electronic circuits [1], sensors [2] and light emitters [3]. Nanomaterials such as inorganic single crystalline nanowires offer both high charge carrier mobilities [4] and solution processability [1] [2] [5]. Following nanowire growth, they can be dispersed in organic solvents and then used as semiconductor inks for low-temperature device fabrication [1] [5] [6]. Silicon nanowires (Si NWs) are particularly attractive due to well-studied Si properties, including high carrier mobility, and also chemical stability of Si with native oxide surface layers. Si nanowires growth methods such as chemical vapour deposition [7] and vapour-liquid-solid growth [8] can produce high quality nanowires, with well-defined nanowire dimensions with few tens of nanometers in diameter and few to tens of microns in length. However, growth throughput is typically limited to the size of the substrate and the length of growth process. Korgel's group [6] has demonstrated that the supercritical fluid liquid solid (SFLS) method for growing Si nanowires can be industrially scalable, with a throughput of up to few kg per day, thus opening opportunities for nanowire synthesis suitable for future printable nanowire electronics fabrication.

One of the key challenges in nanowire device fabrication is the reduction of surface trap states, which can dramatically reduce device performance. Nanowires possess high surface area, and charge transport in nanowire field-effect transistors is strongly affected by the quality of semiconductor/gate-dielectric interface, due to the trapping of charge carriers. Commonly used gate dielectric for Si NW FET fabrication is thermally grown SiO₂. However, SiO₂ dielectric is well known to contain surface bound hydroxyl (OH⁻) groups, where hydrogen is strongly bound to the silanol groups on SiO₂ surface [9][10][11]. The presence of such species on the SiO₂ surface induces interface states that can trap accumulated charges, resulting in current-voltage characteristics instabilities and reduction of charge carrier mobility. The trapping of charge carriers is typically manifested as hysteresis behavior during transistor operation. Hysteresis is the shift in threshold voltage (ΔV_{th}), which can reach up to tens of volts, during the forward (e.g. +V to -V for p-type transport) and the reverse gate voltage sweep (-V

1. Introduction

Solution-processed printable electronics using semiconducting inks have opened up the possibility of various low-cost electronic devices for large area

to +V) at constant drain voltage bias.

Elimination of hysteresis in a transistor device will improve the overall device performance including the effective device field effect mobility, due to less scattering of charge carriers, and will provide more stable current-voltage characteristics. Passivation of devices with poly (methyl methacrylate, PMMA) on PbSe nanowires [10] or self-assembled monolayers (SAMs) on Si NWs was shown to reduce the surface bound hydroxyl group, thereby reducing the hysteresis [11]. Passivation against OH⁻ groups using hydrophobic fluorocarbon encapsulation has also been demonstrated in literature to reduce hysteresis in carbon nanotube FETs [12]. It has also been reported that SiO₂ thermally grown at high temperatures (~1100°C) on Si NW reduces the hysteresis in Si NW FETs [13][14], but such high temperature treatments are too extreme for printed electronics approach. A solution based method offering mild oxidation of Si nanowire shell has also been recently reported, which has led to a reduced hysteresis in Si NW FETs [15]. Gate dielectrics which have lower affinity towards OH⁻ groups such as *a*-SiN_x dielectrics have shown increased mobility in *a*-Si thin film transistors due to less interface charging [16], but the high temperature required for the deposition of the *a*-SiN_x (~250°C - 450°C) makes it incompatible with printed electronics substrates, such as plastics.

However, low-*k* dielectrics such as polymers, have surfaces with low energy disorder, and have been successfully used in organic field effect transistors with high mobility and low hysteresis [17]. Thus, polymer dielectrics, especially hydrophobic fluoropolymers, are strong candidates for nanowire field-effect transistor applications.

In this work, we studied the effect of nanowire –dielectric interface on hysteresis in Si NW field-effect transistors with channel consisting of multiple nanowires by directly comparing SiO₂ and polymer dielectrics interfaces in the same dual-gate FETs. Comparison of separate NW FETs with different dielectric layers is problematic due to challenges in depositing exactly the same number of nanowires with identical properties in the FET channels. Thus, dual-gate NW transistors with bottom SiO₂ and top

polymer dielectrics provide ideal device structures to study the effects of dielectric interfaces on the transistor performance, especially hysteresis, when devices are operated in either top- or bottom gate mode. By directly comparing dual gate nanowire FET operation using bottom SiO₂ gate dielectric accompanied by high current hysteresis of about 30V, with operation using top hydrophobic polymer gate dielectric and much lower hysteresis of only 6 V, we clearly demonstrate the performance advantages of the polymer dielectric. Additionally, we show that Si NW FET performance in bottom gate mode with SiO₂ dielectric cannot be noticeably improved by an encapsulation with polymer layers, further highlighting the importance of the correct nanowire-dielectric operational interface for high performance nanowire devices. These studies directly demonstrate the superior performance of fluoropolymer gate dielectric for nanowire -based FETs.

2. Experimental Details

Silicon nanowires used in this work were synthesised by the supercritical-fluid liquid solid method, as described elsewhere [6]. The formulations of Si NWs dispersed in anisole were used to prepare samples for Scanning Electron Microscope (SEM) and Transmission Electron Microscope (TEM) analysis by drop casting a small amount of dispersion on Si/SiO₂ substrates and on holey-carbon grids (Agar Scientific), respectively. SEM images of as-grown Si nanowires were used to evaluate the NW lengths to be from 2µm to 100µm. Most of nanowires were within 5-30µm length range. Figure 1(a) shows TEM image of a network of Si nanowires with a noticeable amount of impurities, nanowire aggregates and defective kinked nanowires. High resolution TEM in Figure 1(b) shows a typical straight single nanowire with a diameter of ~35nm surrounded by a 4nm thick amorphous shell. The nanowire growth direction was identified from computed Fast Fourier Transform (FFT) pattern obtained from the lattice fringes (Fig. 1(b)) to be along [110], which is consistent with previous reports [6].

Figure 1. (A) TEM secondary electron image of a network of SFLS-grown silicon nanowires showing particles and clumps of nanowires. Carbon TEM grid is visible on the background. (B) High resolution TEM image of a single crystal core nanowire with a 4nm amorphous shell around the nanowire, with the inset illustrating corresponding Fast-Fourier Transform of the image showing the growth direction [110].

Nanowires were deposited on Si/SiO₂ substrates using a roll-cast coating method. The nanowire formulation was drop-casted on the part of the inclined substrate, and a glass roller was placed at the top of the substrate and then allowed to roll down under the influence of the gravitational force. The roller was making contact with the substrate, enabling to spread out the nanowire formulation and to remove protruding clumps, stacked nanowires and large impurity particles. Additionally, the shear force induced by the roller movement was acting on nanowires to produce preferential alignment along the rolling direction (Supporting Information, Fig. S1). The nanowires density on the substrate can be increased by repeating the process, until the required density is achieved. The nanowire alignment can be improved by using a compressed air gun to dry the solvent immediately after the roll-casting process. Following the nanowire deposition the substrates were dried and prepared for photolithography.

For dual-gate FETs, the source-drain electrodes were patterned using photolithography on top of the aligned nanowires by sputtering Au/Cr (50nm/3nm) contacts on Si/SiO₂ wafers and then conducting lift-off process. The substrates were annealed at 200°C in N₂ filled glove box after patterning source/drain contacts, to improve charge injection/extraction. A 1µm thick layer of fluoropolymer (Cytop) was spin coated on top of the substrates and then baked at 100°C for 10min. A 50nm thick Au gate electrode was evaporated through a shadow mask on top of the channel area covered with Cytop. For encapsulation studies, bottom gate NW FET structures with aligned nanowires and photolithographically defined electrodes were coated with two types of polymers including poly (methyl methacrylate) (PMMA ~ MW 120000) and Cytop as follows. 4 wt% solution of PMMA in anisole was spin coated on top of the Si NW FET on Si/SiO₂ substrates and baked at 220°C for 30min inside N₂ filled glove box, resulting in ~600nm thick layer. A 1µm thick layer of Cytop was deposited by spin-coating. Transistor characterisation measurements were performed with Agilent 4155C semiconductor analyzer in N₂ filled glove box to minimize the effect of atmospheric

contamination.

3. FET Results and Discussion

3.1. Effect of Nanowire/Dielectric Interfaces on the Hysteresis

The trapping at the nanowire/dielectric interface plays a crucial role in the transport of charge carriers. The direct one-to-one comparison of the effect of NW-dielectric interfaces on device performance with different organic and inorganic dielectrics is not possible by fabricating separate transistors due to the differences in nanowire numbers present in the FET channels, and also due to possible variation in nanowires' properties including diameters, shell thicknesses, levels of impurities, and Si core growth directions, resulting from non-uniform characteristics of as-synthesised SFLS nanowires[5][6][18]. Instead, we have fabricated double gated transistors with two different dielectrics interfacing the same nanowires. The nanowires forming the FET channel were gate biased through the bottom SiO₂ dielectric, and, in a separate set of tests, were top-gate biased through the Cytop dielectric. These dual-gate structures allowed us to eliminate the variation of Si NW morphology, placement position and the number of nanowires for the comparative studies of hysteresis effects in SiO₂ vs organic dielectric interfaces. Figure 2 shows the transfer and output characteristics of a typical double-gate Si NW transistor with SiO₂ as bottom-gate dielectric and Cytop as top-gate dielectric, with 23 nanowires bridging the channel. Both the bottom gate and the top gate measurements demonstrated good channel modulation, with p-type accumulation behavior, with an I_{ON}/I_{OFF} ratio of ~ 10⁶ for the bottom gate bias mode and >10⁶ for the top gate bias mode. (I_{ON}/I_{OFF} and hysteresis extraction are described in Supporting Information, Fig.S2). The devices showed a near-Ohmic contact behavior, as observed in the output characteristics in Figure 2 (b, c).

Figure 2. Transfer and output characteristics of a typical double gate Si NW FETs with SiO₂ bottom gate dielectric and fluoropolymer top gate dielectric: (a) transfer plots measurements in top gate and bottom gate modes ($V_D = -5V$), arrows show the direction of gate voltage sweep; (b-c) output characteristics for bottom gate and top gate modes obtained by scanning drain voltage from 0 to -6V and measuring the drain current at constant gate voltages [$V_G = -20V, -30V, -40V, -50V, -60V$].

Operation of the FET in the bottom gate mode with Si nanowires/SiO₂ interface results in large hysteresis (ΔV_{th}) is about 31V (Fig.2a). However, the hysteresis (ΔV_{th}) obtained by gating only the top organic dielectric interface gives much lower hysteresis of only ~ 6V, which we attribute to lower trap density at the NW hydrophobic polymer dielectric interface, as we discuss in more details later on.

A higher I_{ON} at $V_D \sim -5V$ was observed for the bottom gate SiO₂ measurements as compared to the top gate organic dielectric scans, due to higher dielectric constant value ($\epsilon_{ins}=3.9$) and lower thickness (230nm) of the SiO₂ insulator vs corresponding values for Cytop ($\epsilon_{ins}=2.1$ and 1 μm thickness).

We can further analyze the data by comparing charge carrier mobilities and trap densities for SiO₂ and Cytop interface measurements. For calculating the nanowire FET mobility, parasitic capacitance and fringing of the gate field due to the cylindrical nature of the nanowires should be taken into consideration. The nanowire FET mobility equation in the linear regime is given below [1] [19] [20]:

$$\mu = G_m \times \frac{L^2}{V_D C_n} \quad (1)$$

$$C_n = N \times \frac{2\pi\epsilon_o\epsilon_{ins}L}{\cosh^{-1}\left(\frac{r+d}{r}\right)} \quad (2)$$

Here C_n is the capacitance based on cylinder on a plate model for N number of nanowires in the FET channel with radius r and gate dielectric thickness d , G_m is transconductance ($G_m = \partial I_D / \partial V_g$), L is the channel length,

ϵ_o is the absolute permittivity, ϵ_{ins} is the gate insulator dielectric constant and V_D is the drain bias voltage. A capacitance of $\sim 7.2 \times 10^{-15}$ F was calculated for Si-NW FETs on SiO₂ using equation (2), whereas capacitance of Si-NW/Cytop structure was $\sim 2.5 \times 10^{-16}$ F. From equation (1), the extracted Si NW FET mobility of the top gate Cytop interface was found to be 12 cm²/Vs, and it is significantly higher than mobility extracted for the bottom gate SiO₂ interface of 1.7 cm²/Vs. The enhanced mobility for the top gate device can be attributed to the less scattering from trapped charge carriers in the Si NW/polymer dielectric interface.

Based on the hysteresis values (ΔV_{th}) we have evaluated the occupied trap density at the nanowire-dielectric interface related to the hysteresis using the following equation [11]:

$$NqQt = \frac{C_n \times |\Delta V_{th}|}{2\pi rL} \quad (3)$$

Where, q is the elementary charge and Q_t is the occupied trap density. Other notations are defined in Eq. 1-2. Typical radius (r) of Si nanowires is $\sim 20nm$ ($\pm 5nm$) and the nanowire length is estimated as the channel length (5 μm) of the dual gate FET.

For the bottom gate SiO₂ interface, Q_t was evaluated to be $\sim 1 \times 10^{13} \text{ cm}^{-2}$ which is more than an order of magnitude higher as compared to the Si NW/Cytop top gate interface with $Q_t \sim 7.5 \times 10^{11} \text{ cm}^{-2}$. This difference shows that the organic dielectric forms a higher quality lower-trapping interface as compared to the SiO₂ interface.

Figure 3. Transfer characteristics of bottom-gate (SiO_2 dielectric) silicon nanowire FETs before and after capping with polymer layers, measured in N_2 environment: (a) hysteresis $\Delta V_{\text{th}} \sim 23\text{V}$ before PMMA coating, and $\Delta V_{\text{th}} \sim 19\text{V}$ after PMMA coating; (b) hysteresis $\Delta V_{\text{th}} \sim 33\text{V}$ before Cytop coating, and $\Delta V_{\text{th}} \sim 31\text{V}$ after Cytop coating.

This section can be concluded by the following observation: key nanowire transistor parameters, such as hysteresis, charge carrier mobility and interface trap density are all consistently improved by changing the operational nanowire dielectric interfaces from SiO_2 to fluoropolymer Cytop. Hydrophilic SiO_2 interface has high affinity for surface bound OH^- groups, serving as trap sites for charge carrier, as reported in the literature, whereas hydrophobic low- k Cytop polymer, on the contrary, has very low affinity for hydroxyl ions, thus providing low-trap dielectric interface to the semiconducting channel, resulting in lower trap density, higher mobility and lower hysteresis for nanowire FETs.

3.1. Effect of Capping Layers on Hysteresis in SiO_2 Bottom Gate Transistors

To investigate whether organic capping layers can affect the hysteresis in Si-NW FETs gate-biased exclusively through SiO_2 bottom gate dielectric, we have fabricated nanowire transistors with PMMA and Cytop encapsulation layers, as described in section 2. The question that we have tried to answer is how much these capping layers can affect charge transport characteristics at the bottom nanowire- SiO_2 interface.

Figure 3 shows transfer characteristics of Si-NW FETs with SiO_2 as gate dielectric before and after encapsulation with two polymers, PMMA and Cytop. The devices were measured in dry nitrogen conditions to minimize the effects of atmospheric contamination.

The drain current (I_D) was measured by scanning the gate voltage from $+20\text{V}$ to -60V in the forward voltage sweep and from -60V to $+20\text{V}$ in the reverse voltage sweep, at -6V drain bias voltage (V_D). The gate voltage sweep rate was kept constant at 1V/s throughout the measurements.

From the transfer characteristics in Figure 3(a) for a PMMA coated device, a p-type behavior is observed showing charge accumulation at negative bias gate voltages,

similar to measurements in the previous section. The device showed good gate modulation with an $I_{\text{ON}}/I_{\text{OFF}}$ ratio of $>10^6$ (forward scan) and a threshold voltage of $\sim -16\text{V}$ before PMMA coating (see Supporting Information Fig.S2 for V_{th} extraction). The hysteresis (ΔV_{th}) was extracted by taking the difference of threshold voltages obtained from forward gate sweep and reverse sweep. A hysteresis of $\sim 23\text{V}$ was observed for the open surface (uncoated) Si NW FET device. Upon PMMA coating, a small negative shift in the threshold voltage to $\sim -23\text{V}$ was observed, and hysteresis (ΔV_{th}) was found to be $\sim 19\text{V}$. This value is smaller than that of un-coated devices, possibly indicating that carboxyl groups in PMMA might have removed some of surface bound OH^- groups, similar to the process reported for PbSe nanowires [10]. However, the value of hysteresis in PMMA coated Si NW FETs is still quite large.

In the other set of samples, the nanowire transistor performance was compared before and after Cytop coating, as shown in Figure 3(b). Threshold voltage and hysteresis before fluoropolymer coating were found to be $V_{\text{th}} \sim -3\text{V}$ and $\Delta V_{\text{th}} \sim 33\text{V}$, respectively. After Cytop coating, the threshold has shifted slightly positive to 3V , and hysteresis has moderately reduced to 31V . As the hysteresis changes after polymer coatings were found to be relatively small, it was concluded that charge transport at silicon nanowire/ SiO_2 dielectric interface is mainly governed by the nature of the operational interface itself, and is only marginally affected by the capping polymer layers.

4. Conclusions

Examination of experimental results of dual gate Si NW FETs operated in bottom SiO_2 gate mode and a fluoropolymer top-gate mode, and results for bottom gate FETs with two polymer capping layers, PMMA and Cytop, point to the following conclusions. Charge transport in nanowire FETs is directly affected by the

semiconductor/dielectric interface, which provides a high degree of control of charge interface traps. As demonstrated in this work for identical silicon nanowire FET channel, switching from SiO₂ dielectric interface to hydrophobic fluoropolymer interface provided over an order of magnitude reduction in surface trap density Q_{it} , from $\sim 1 \times 10^{13} \text{ cm}^{-2}$ to $7.5 \times 10^{11} \text{ cm}^{-2}$. Importantly, Cytop top gate interface operation demonstrated 7 times increase in mobility and 5 times lower hysteresis as compared to bottom Si/SiO₂ interface operation. Capping of bottom gate SiO₂ silicon nanowire transistor devices with polymer layers such as PMMA and Cytop, while keeping the SiO₂/nanowire operational interface, provided only minor improvement of hysteresis.

These results demonstrate that hybrid device fabrication approach, combining solution processed inorganic semiconducting nanowire transistor channel with low-polarity fluoropolymer gate dielectric layer, provides optimum NW FET device structure, fully compatible with printed electronics fabrication methods.

Small nanowire footprint, high mechanical robustness, high charge carrier mobility, low temperature device processability open a number of applications for nanowire transistors, including flexible circuits, tensile sensors for robotic skin, optoelectronic detectors, rollable displays and nonvolatile memory devices.

Supporting Information

Deposition and alignment of silicon nanowires with a roll-cast method

Figure S1. Polarised optical microscope images of SFLS grown silicon nanowires on Si/SiO₂ substrates: (A) nanowires deposited by drop-casting, with substrate in an inclined position to allow gravity assisted formulation flow. Most of nanowires are not aligned. Only few wires are aligned according to the flow direction; (B) example of non-aligned nanowires, with clumps of nanowires on the substrate after drop-casting deposition, (C) and (D) roll-cast aligned nanowires with no clumps of nanowires/particles, arrow represents the direction of alignment (roller movement); (C) lower magnification, (D) higher magnification of the same area.

Figure S2. Linear regime transfer characteristic of a typical Si-NW FET in a linear and a log-linear scale. Forward V_g scan is from +20V to -60V, immediately followed by a reverse V_g scan from -60V to +20V. Hysteresis ΔV_{th} is extracted from the linear plot by taking the difference between the threshold voltages for the forward and for the reverse scans. Threshold voltage is defined as intersect of a linear fit to the I-V curves and the zero-current axis. I_{ON}/I_{OFF} current ratio is extracted from the log plot, by taking the ratio of maximum current obtained during accumulation and the current when the FET is in the ‘off’ state.

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