Validating Some Signal Integrity Procedures for Transmission of Digital Signals on Microstrip Circuits

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Abstract Because of the high volume of processing, transmission, and information storage, electronic systems presently require faster clock speeds to synchronize the integrated circuits. At present the “speeds” on the connections of a printed circuit board (PCB) are up to 4 GHz or even faster. At these frequencies the behavior of the interconnects are more like that of a transmission line, and hence distortion, delay, and phase shift-effects caused by phenomena like cross talk, ringing, and overshoot are present and may be undesirable for the performance of a circuit or system. Thus, the interconnects do not have to be considered like simple conductors or lumped elements. All this gives rise to a new emerging discipline known as signal integrity. In this discipline the correct timing and signal quality preservation preventing transients and false switching are studied in order to avoid excessive delays. These phrases were extracted from the chapter eight of book “2-D Electromagnetic Simulation of Passive Microstrip Circuits” from the corresponding author of this paper.

Keywords Signal Integrity, Transmission Lines, Distortion, Delay, Phase Shift-Effects, Cross Talk, Ringing, Overshoot, Transients, False Switching, Timing, Signal Quality.

typical lossy transmission line, has a lumped element equivalent circuit given by a ladder network composed of repeated L, T, or Π sections of resistive (R), inductive (L), capacitive (C), and conductive (G) elements.

Figure 1. Behaviour of the transmission of the amplitude and angle of a synchronous impedance transformer

1. Introduction

This paper compares the transmission characteristics of a synchronous impedance transformer given in [1] with those of a sequential impedance transformer given in [2]. The comparison is presented by considering the resistive losses, the dielectric losses, the radiation losses and the discontinuities. Also, both structures were compared with two different techniques:

One of these techniques is to analyze the equivalent circuit based on the transmission line theory, because as a physical element, a transmission line can transmit, dissipate and store energy. Thus for instance, a two-wire line, which is a

Figure 2. Behaviour of the transmission of the amplitude and angle of a sequential impedance transformer

The other technique is the application of the FDTD (Finite Difference Time Domain) method to simulate electromagnetic phenomena, the FDTD starts with a discretization of the equations that model the phenomena. In this case, a pair of differential equations that are solved for staggered time and space interval. This mathematical discretization conveys a physical segmentation of the structure on study where the segmentation can be performed using cells of equal and different sizes [1].

As mentioned in [2], the resistive losses (I^2R) are due to the finite conductivity of any metal. In addition, as frequency increases, skin effect confines the currents to a smaller portion of the metal thickness, increasing the effective resistance and corresponding loss.

The dielectric losses are the additional losses caused by the reduction in velocity of the signal, plus any energy absorbed by the dielectric material. The apparent increase in conductor length increases the loss as if the conductor were physically longer.

In a closed system, such as a coaxial cable, radiation losses are small, but as shown in Figure 3, circuit and package conductors more closely resemble microstrip when they are single conductors over a ground plane, stripline when they are embedded between "ground" layers of a p.c. board, parallel lines in air or dielectric, or conductors passing through layers. These transmission line structures allow coupling to adjacent conductors and components via the electric and magnetic fields, as well as radiation (and reception) like antennas.

The coupling and radiation noted above give rise to crosstalk, where energy from one signal line is transferred to another line. Just like interference in the radio environment, excessive crosstalk can impair the quality of the desired digital signal.

Figure 3. Signal path conductors in electronic circuits are transmission lines, may have any of above configurations

Time delay Delay-Any conductor requires a certain amount of time for a signal to travel from one end to another. With a repetitive waveform (e.g., RF sine wave),

that delay can also be characterized as a phase difference between the input and output. With a train of digital pulses, the actual transit time is a more appropriate measure.

Reflection Impedance-is a frequency-domain-bases term, which digital signal engineering has not traditionally used. It is the amplitude of the voltage and current, along with the phase difference, expressed either as a magnitude and angle ($R \angle \theta$) or in Cartesian real/imaginary coordinates ($R \pm jX$).

Characteristic impedance of a transmission line is a function of physical size, nature of the ground, and the intervening dielectric material. For example, narrow p.c. board traces will have a higher impedance than wide traces.

Figure 4. The signal integrity problem: An ideal waveform (top) has variations due to the effects of the signal path, such as the ringing shown in the bottom waveform. Also note that the ringing may reach the HI logic level threshold, causing data errors.

Discontinuities Discontinuities-A mismatch between a device's impedance and the impedance of the transmission line creates a point of discontinuity. These can occur at the device pins, or at any variation in the p.c. trace along its route, such as a bend or transition through a via hole. When the traveling wave meets a discontinuity, a portion of the energy is reflected back toward the source. If there is also a mismatch at the source, a further reflection will occur with energy "bouncing" between discontinuities.

These reflected signals are summed the desired signal, and if large enough can greatly distort the waveform. Minimizing reflections and maintaining an impedance match between source and load is required for robust SI design.

Resonance Resonance-When a reflection has a time delay equal to a multiple of 1/2-wavelength at a corresponding frequency, there is a perfect alignment for partial

cancellation of a signal. This is a critical issue in the time domain, because a digital “square” waveform contains the fundamental clock frequency plus significant energy at several of the odd-numbered harmonics. At resonance at $3\times$ clock frequency will result in a greatly distorted waveform and potential data errors. Because resonance is a function of time, there is no amplitude-based equalization scheme that can remove its effect.

Figure 2 shows some of the reflection effects. At the top is the test circuit, a line section with 50 ohm lines at the input and output, and a section of 25 ohm line placed in the center. The line lengths are chosen so that reflection, mismatch and loss effects can be analyzed over the desired frequency range. The plot shown covers a range of six harmonics of the primary resonance. The deep reductions in amplitude show the signal cancellation, while the overall level falls off with increasing frequency, due to the various loss mechanisms.

The information presented in [2] and reproduced in here, has shown a brief introduction to the physical effects of signals on transmission lines. The original author of [2] manifest hopefully these basics will serve as a foundation for greater understanding of the issues involved in engineering for good signal integrity.

The purpose of the present paper is simply highlight the importance of the different loss factors presented in [2] in order to show the similitudes between the responses of the synchronous impedance transformer given in [1] with those of a sequential impedance transformer given in [2].

As explained in the abstract of [8], the excessive interconnection delay and fast increasing development cost, as well as complexity of the single-chip integration of different technologies, are likely to become the major stumbling blocks for the success of monolithic system-on-chips. To address the above problems, this paper investigates a new VLSI integration paradigm, the so-called 2.5-dimensional (2.5-D) integration scheme. Using this scheme, a VLSI system is implemented as a three-dimensional stacking of monolithic chips. A cost analysis framework was developed to justify the 2.5-D integration scheme from an economic point of view. Enabling technologies for the new integration scheme are also reviewed. Also from [8], the following can be highlighted

2. Background

FUNCTIONALITY increase has been and will continue to be the major driving force for the semiconductor industry. As a matter of fact, the spectacular success of IC industry in the past 30 years depends on the ability to continuously shrink the feature size of IC fabrication process and at the same time pack more devices on a single silicon die. However, when the main-stream fabrication technology is now moving to the 90-nm node, the feasibility of the monolithic integration paradigm is severely stumbled by the following factors.

Interconnection “Crisis”: Historically, functionality to be integrated in a single chip at every technology generation always exceeds the capacity provided by pure scaling. To accommodate the extra transistors, chip size has always been increasing since the invention of the first integrated circuit [1]. The problem is that, interconnection length, especially worst-case interconnection length, has to increase as long as IC chip size is expanding. Starting from the 0.25 μm generation, the interconnection delay of long on-chip wires has become the dominant part determining system performance [2, 4]. As a result, the timing of global signals has become a critical concern. Unfortunately, interconnection delay is very hard to predict before the circuit is actually laid out. As a result, current synthesis-based VLSI design methodology often has difficulty to achieve timing closure.

Fabrication Cost: The extreme complexity of today’s semiconductor process leads to a skyrocketing of the fabrication facility cost [5]. It has been reported that the cost of a single mask set and corresponding probe will soon reach \$1 million [6, 7]. Meanwhile, modern system-on-chips (SoCs), especially those for wireless applications, typically integrates heterogeneous components. These components are originally targeted for different fabrication technologies. This further complicates the merged process and raises fabrication cost. For example, in a RF-CMOS process, the price of a finished wafer is higher than that of pure CMOS by at least 15% [8]. Meanwhile, for RF circuits, it is difficult to achieve further performance improvement and cost reduction by using a scaled technology. For instance, many analog transistors and passive components have to occupy a relatively constant die area to meet performance requirements no matter in which technology generation they are fabricated [8].

Memory Gap: Memory bandwidth has already become the limiting factor impeding the performance of general-purpose microprocessors and multimedia appliances, as well as other data-intensive applications. It has been reported that the processor performance has been improving by 35% annually from 1980 to 1986 and by 55% annually thereafter [9, 10]. In the same period, the access latency of DRAM has been improving by only 7% per year [9]. Now this problem is mainly addressed by introducing cache hierarchy and integrating memories with the logic on the same chip. For most current processors, at least 50% of the die area is occupied by cache memories [11]. Also, a PDA-type phone could use as much as 128-Mb flash and 128-Mb DRAM [12]. Embedded memory requires a merged memory/logic process, which is more expensive and leads to inferior memory devices [13, 14]. Moreover, the long interconnects of the memory buses can also become a bottleneck when a large amount of memory is integrated.

It must be indicated that the above problems are inherent to the monolithic integration. Therefore, the key question must be raised: How to build modern systems that avoid the shortcomings of monolithic SoC, while maintaining momentum in the increase of the functionality?

3. Conclusions

As can be seen by running the routine of [1] (page 61 of that reference), the behavior of both, the synchronous impedance transformer and the sequential impedance transformer show clearly an amplitude downward as the frequency growth to 16 GHz in Figure 1.

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